Microvia Reliability Using a Simple Test Vehicle

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Abstract
Microvia reliability is dependent on many factors including: dielectric mechanical properties, crystal size, shape, thickness and orientation of the copper grain metallization, microvia design, stacking or staggering, layer count, degree of offset, aspect ratio, the presence of a thick subassembly, cap plating thickness, and fabrication defects. A 47 mil thick layer of FR4 was used as a subassembly where a single 4 – 5 mil microvia was placed above and below the subassembly with no offset between the microvia and the epoxy filled, mechanically drilled subassembly. The microvias were constructed from a unreinforced, fiberglass free dielectric having a Z axis coefficient of thermal expansion of ≤ 30 ppm/◦C (RT to 260◦C). The epoxy filled plated through hole in the subassembly puts an enormous amount of stress on microvias. The reliability of CITC and D-coupons was investigated when the coupons were thermocycled to 260˚C. A second goal was to evaluate coupon reliability across four different PWB fabricators to correlate microvia reliability to fabricator capability. Failure analysis was done after thermocycling to understand the relationship between failure defects and 260˚C thermocycling. Lastly, using stress analysis, the theoretical reliability of the test coupons was predicted using commercially available software based on coupon mechanical properties. This study uses an unreinforced dielectric that has thermal expansion characteristics close to copper such that little stress is generated between a thermal mismatch of the copper to the dielectric, allowing the performance of the coupons to be correlated to coupon fabrication.

Introduction

Printed circuit density is only increasing with a greater incorporation of microvia structures. The next 5 years are expected to show a 50% increase in HDI manufacturing even in North America. Unreinforced build-up materials are common in semiconductor packaging and commercial applications such as cellular phones but are being driven into many more industries. The driver in semiconductor packaging is heterogeneous packaging incorporating chiplets where all types of devices can be included within the packaging: high band width memory, flash memory, MEMS, processor/logic/system on chips/specialized processors, AiP, filters, capacitors, inductors, resistors, RF chips, sensors. The prepreg or build-up material has to serve many functions in today's advanced designs (1) compatibility with almost no profile copper (adhesion thereto) or yield acceptable peel strength after sputtering (2) flexible and available in roll form for hot roll lamination (3) has to flow and fill difficult copper artwork where the copper may have been plated up to 1-2 mils – needs low viscosity for advanced designs (4) have low CTE matched to copper for thermal reliability (5) should have low loss (DF) and low DK for today's high speed digital applications (6) should serve as a leveling agent to yield a flat surface for semiconductor attach (7) should be compliant and not crack for increasingly larger semiconductors (8) should be lower modulus and less prone to cause warpage in large semiconductor packages (9) in hybrid stack-ups needs to bond and not delaminate from very difficult materials such as polyimide, LCP, low CTE ceramic loaded substrate cores.

The future of semiconductor packaging is increased densification where the build-up material may not be combined with substrate cores based on fiberglass and epoxy. The build-up material will be thinner and thinner and will likely be combined with glass cores that are used to control the warpage in increasingly larger semiconductor packages.

Commercial applications employing build-up where the layers are thin and the overall pwb is thin and there is no "subassembly" in the middle of a PWB have less of a reliability challenge than military, space, and avionics applications where there could be one or more subassemblies built in the design. Thermal reliability takes on a much more critical role in military, space, and avionics applications such that RF and digital designers are handicapped or completely restricted with regard to how they can design and layout a PWB regardless of how it influences the electrical performance. PWB reliability, PWB manufacturability, and PWB reproducibility dictate how and what an engineering team can design in military, space, and avionics. The challenge is that semiconductors are getting more advanced and need higher levels of circuit routing. Specialty processors will reach 7–10 layers of build-up material on each side of a substrate core or glass core material. Overall build-up layers will reach 14–20 layers. Because military and avionic applications are low volume, designers of military, space, or avionic hardware are sometimes forced to use the advanced semiconductors from the commercial market. Heterogeneous packaging is not new to military, space, and avionic applications. However, these types of applications require unique designs where engineers prefer not to use off the shelf commercial semiconductors and packaging. The pressure for incredible levels of densification is increasing not just on the large OEMs building advanced processors for gaming, AI, high speed computing, 5-6G wireless, it is putting pressure on the companies that build the world's best military hardware. Asymmetric technology in warfare is a term used to describe being one generation ahead of your opponent such that in a military conflict your technology wins because it has a one generational development cycle advantage vs your opponent. Commercial companies always seek this one

generational advantage. Semiconductors are reaching their limitations based on physics. Semiconductor packaging needs to keep up with semiconductor design, not be the weakest link or limiting factor and unreinforced build-up material is critical for that progression.

Reliability criterion cannot get relaxed or compromised. Electrical performance will not get compromised. Future demand calls for materials with a dk = 2.0 – 3.2 with a DF ≈ 0.002 with suitable thermal reliability for any number of build-up layers. Through via and microvia reliability are commonly tested by various methods: Please see IPC Methods: IPC-TM-650 TM 2.6.26[1] (CITC), IPC-TM-650 TM 2.6.27[2] (D-coupon testing) IPC-TM-650 TM 2.6.7.2[3] (6X solder reflow testing). Interconnect stress testing (IST) is also a valuable test for measuring reliability and can be used to predict the lifetime of product. The debatable limitation of IST is that the coupon generally reaches up to 190˚C and does not test to lead free reflow temperatures. CITC (Current Induced Thermal Cycle) is an alternative method advanced by IBM Endicott to try to predict reliability based on stressing the via structures to solder reflow temperatures. The IST method uses lower temperatures to predict product life and the CITC method uses more extreme solder reflow temperatures to predict product life. Regardless of the method, it has been a general practice of defense, space, and aerospace industries to prohibit designers from using a certain number of stacked microvias and to prohibit designers from placing a stacked microvia directly over a thick subassembly with no offset. Both D-coupons and CITC coupons can be readily incorporated into production product to verify the quality of every lot or panel manufactured. To compare relative performance of materials, a test vehicle such as the test vehicle shown in Figure 1 can be used to rank materials and their robustness in microvia designs[4]. Typically, a 47 mil thick FR4 is used as a subassembly. The dielectric material under test is 4-5 mils but can be thinner or thicker. A standard FR4 epoxy will have a mediocre glass transition and a fairly high expansion rate above Tg, a CTE from 2.5-3.0% over the range of RT to 260˚C. The FR4 material will undergo a lot of expansion and put stress on the single microvia layers. At first glance this simple design does not look like it would create a lot of stress on the top and bottom microvias. Surprisingly, when a standard FR4 is used in the subassembly and a standard FR4 is used in a surface microvia layer, the reliability is poor. This type of information and a library of relative material performance is proprietary. A standard hybrid PWB with a much thinner subassembly would put a lot less stress on a single microvia. Therefore, it would take many more reflow thermocycles to establish relative performance of materials. If a single microvia were staggered or offset to the subassembly, then the resulting stresses in the Z axis would be decoupled and only a single level of microvia reliability would be measured. The design in Figure 1 is very interesting because the stress in the Z axis through the epoxy filled mechanically drill subassembly is coupled and compounded with the stress on the microvia and one could vary the thickness of the subassembly to reach a high enough stress level to acquire data quickly. If the stress level is too low, then it would take an infinite number of cycles to draw conclusions on relative performance. If the subassembly were too thick and everything fails quickly immediately, then one cannot draw conclusions as to the relative reliability of a variety of materials. The subassembly needs to be thick enough such that poor materials like FR4 fail quickly, average materials don't fail immediately and really good materials that shine in performance take a lot of reflow thermocycles to fail (25-50 reflow cycles at 260˚C, for example). It should also be noted that microvia size and aspect ratio are key variables. A microvia with a 5 mil diameter and aspect ratio of 1.0 has been chosen for this study.

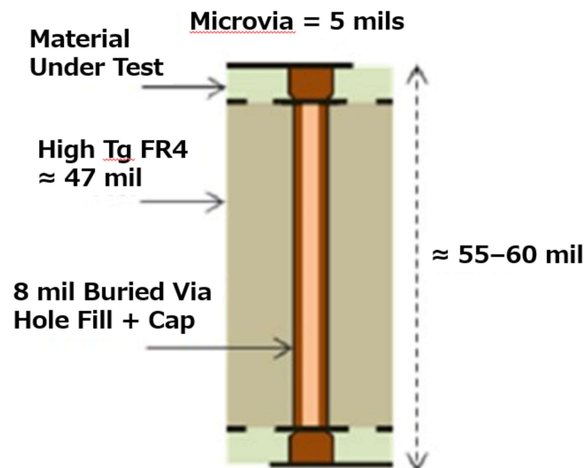


Figure 1 - Standard test vehicle to measure relative material performance of a single microvia top and bottom of a thick subassembly.

Objectives

A. Use an unreinforced build-up film with low CTE to investigate how it would perform in a CITC coupon/D-coupon constructed according to Figure 1.
B. Model/simulate the expected microvia reliability using commercially available stress analysis software
C. Fabricate the coupons at 4 different North American fabricators to try to correlate the CITC/D-coupon performance with the presence of any fabrication defects.
D. Perform failure analysis on coupons of interest
E. Use FIB, SEM, or other tools to try to correlate the electroless copper layer (size, thickness, orientation etc) with the observed coupon reliability with respect to "infant mortality defects" (thermocycles failing in the 1st or 2nd reflow associated with a fabrication defect).

Test Vehicle Design

The basic properties of the unreinforced build-up film used to manufacture the microvia layers of the coupons are as follows: Dk = 3.20, Tg = 175, 261 by TMA, CTE = 29 ppm/C (RT to 260˚C). The CITC and D-coupons are shown in Figure 2. The Z axis CTE (RT to 260◦C) of the coupons built by the four fabricators were as follows: Fabricator 1 – 2.03%, Fabricator 2, 2.32%, Fabricator 3 – 2.1%, Fabricator 4 – 1.7%.

FR4-epoxy typically has a Z axis expansion of 2.5 – 3.0% over the temperature range of RT to 260◦C. The FR-4 material used in this research has a Z axis expansion of 2.8% from 50-260°C. This suggests that the low Z axis expansion of the unreinforced build-up film did lower the overall pwb Z axis expansion. Fabricator 4 used some of the unreinforced build-up film in the subassembly and this appears as a lower overall Z axis expansion.

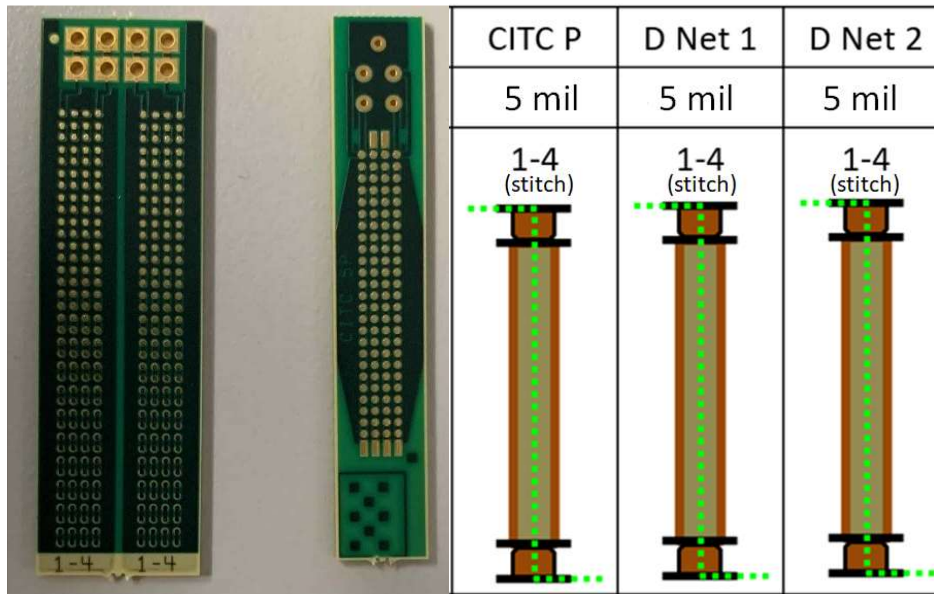
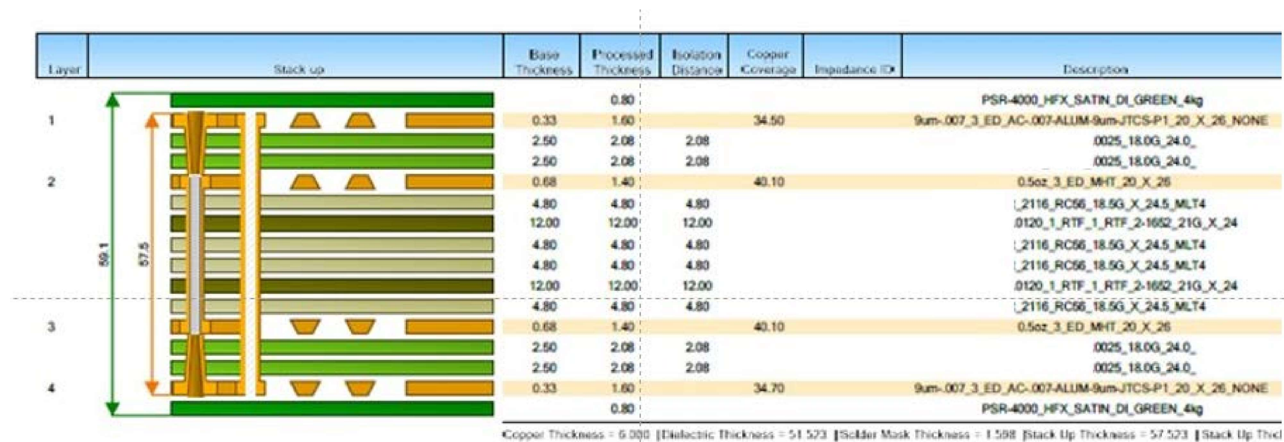


Figure 2. From left to right is the D-coupon, the CITC-P coupon, and the stitching of both coupons from layers 1 – 4 with no offset to the buried subassembly.

The stack-up followed by most fabricators is shown in Figure 3



Layer	Stack up	Base Thickness	Processed Thickness	Isolation Distance	Copper Coverage	Impedance ID	Description
			0.80				PSR-4000_HFX_SATIN_DI_GREEN_4kg
1		0.33	1.60		34.50		9um-.007_3_ED_AC-.007-ALUM-9um-JTCS-P1_20_X_26_NONE
		2.50	2.08	2.08			.0025_18.0G_24.0_
		2.50	2.08	2.08			.0025_18.0G_24.0_
2		0.68	1.40		40.10		0.5oz_3_ED_MHT_20_X_26
		4.80	4.80	4.80			_2116_RC56_18.5G_X_24.5_MLT4
		12.00	12.00	12.00			.0120_1_RTF_1_RTF_2-1652_21G_X_24
		4.80	4.80	4.80			_2116_RC56_18.5G_X_24.5_MLT4
		4.80	4.80	4.80			_2116_RC56_18.5G_X_24.5_MLT4
		12.00	12.00	12.00			.0120_1_RTF_1_RTF_2-1652_21G_X_24
		4.80	4.80	4.80			_2116_RC56_18.5G_X_24.5_MLT4
3		0.68	1.40		40.10		0.5oz_3_ED_MHT_20_X_26
		2.50	2.08	2.08			.0025_18.0G_24.0_
		2.50	2.08	2.08			.0025_18.0G_24.0_
4		0.33	1.60		34.70		9um-.007_3_ED_AC-.007-ALUM-9um-JTCS-P1_20_X_26_NONE
			0.80				PSR-4000_HFX_SATIN_DI_GREEN_4kg

Copper Thickness = 6.000 | Dielectric Thickness = 51.523 | Solder Mask Thickness = 1.598 | Stack Up Thickness = 57.523 | Stack Up Thic

Drill Image	1st Layer	2nd Layer	Drill Type	Fill Type	Minimum Drill Size	Minimum Pad Size	Data Filenames	Column Position	Mu La
	1	2	Laser PTH	Copper Fill	5.00	18.00		1	
	1	4	Mechanical PTH	None	23.60	50.00		2	
	2	3	Mechanical PTH	Non-Conductive	7.90	18.00		1	
	4	3	Laser PTH	Copper Fill	5.00	18.00		1	

Figure 3 Stack-up and manufacturing details used by most fabricators building the CITC-P/D-coupons unless they requested exceptions

Simulated Performance of Hybrid Stack-ups

One objective of the research was to simulate the results using commercially available modeling software for microvia reliability[5]. The software requires the following ***room temperature*** material inputs to model the stress in a given HDI construction: tensile modulus, density, Poisson's ratio, CTE above and below the stated glass transition. The PWB stack-up needs to be defined with the number of layers, the copper weight and retention of copper, the thicknesses of the various dielectrics, configuration of vias (stacked or staggered), pitch (1 mm), via diameter (5 mil), whether a buried subassembly is copper/epoxy filled or not. The dielectric thicknesses in the HDI layers were approximately 4.8 mils. Reflow temperatures were set at 260˚C. The rough copper density on each layer can be inputted. The software has some limitations. The software does not capture areas on a circuit board where there are higher and lower concentrations of copper or reflect the artwork. For this reason, the software will not capture any stress concentration. The software does not include the variation in any of the mechanical properties over temperature. The user inputs only room temperature mechanical values. If the tensile modulus drastically increases or decreases during thermal cycling to 260˚C, those changes will not be reflected. This author would argue that the coupons will likely reach their highest stress levels at the elevated temperatures. Therefore, temperature dependency of the mechanical properties is necessary for accurate simulation. While the user should be careful in assuming that such modeling will yield accurate absolute performance, the modeling software is useful to model relative performance. One can have confidence that relative trends can be observed using the software. For example, increasing or decreasing the pitch or increasing or decreasing the dielectric thicknesses will have clear impacts on the stress levels and this can be readily modeled. As a reference, the first material modeled was the FR-4 epoxy material used in the study. FR-4 epoxy material was used as a reference to suggest how a basic FR-4 epoxy material would perform using the CITC-P/D-coupon of this study. The modeling was done using reflow temperatures of 245 and 260˚C. The modeling can be done on layers 1-2 which are mirrored on layers 3-4 only observing the expected reliability of the microvia layers. Alternatively, the modeling can be done through all 4 copper layers. The modeling done for FR-4 reflow at 245 and 260◦C are shown in Figures 4 – 6 respectively. The modeling software predicts that the 100% FR-4 stack-up (the microvia layers only) will survive between 5 and 10 cycles depending on whether the reflow is done at 245 or 260˚C. When the entire stack-up is modeled, the software predicts a poor result around 1 cycle. It should be emphasized that the modeling software does not capture changes in mechanical properties over temperature which could add or detract from the expected reliability performance.

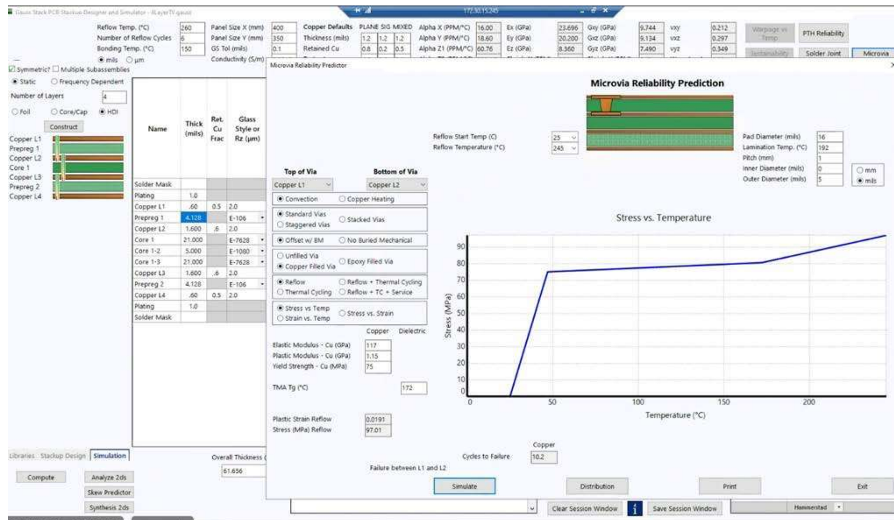


Figure 4 Simulation of solder reflow to 245°C using 100% FR-4 epoxy as the dielectric material modeling only the thermal reliability of layers 1-2

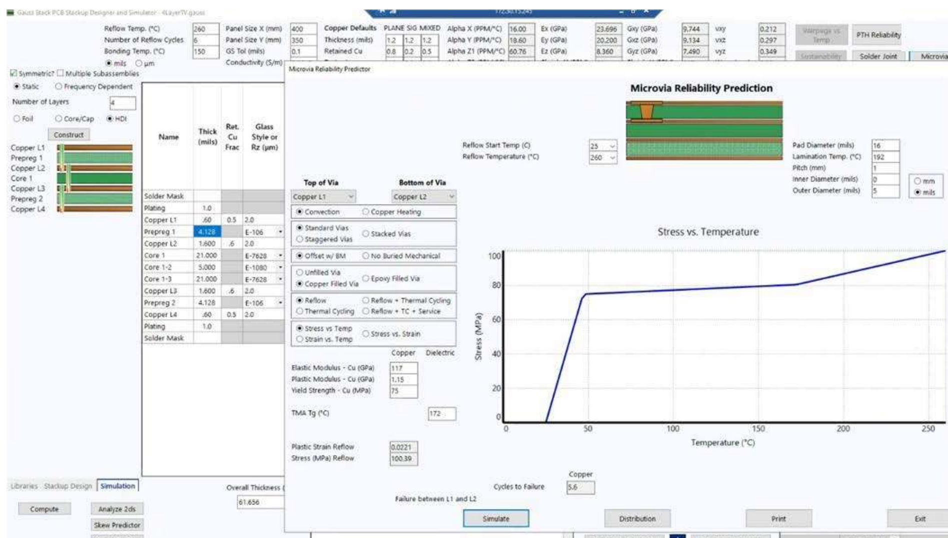


Figure 5 Simulation of solder reflow to 260°C using 100% FR-4 epoxy as the dielectric material modeling only the reliability of microvia layers 1-2

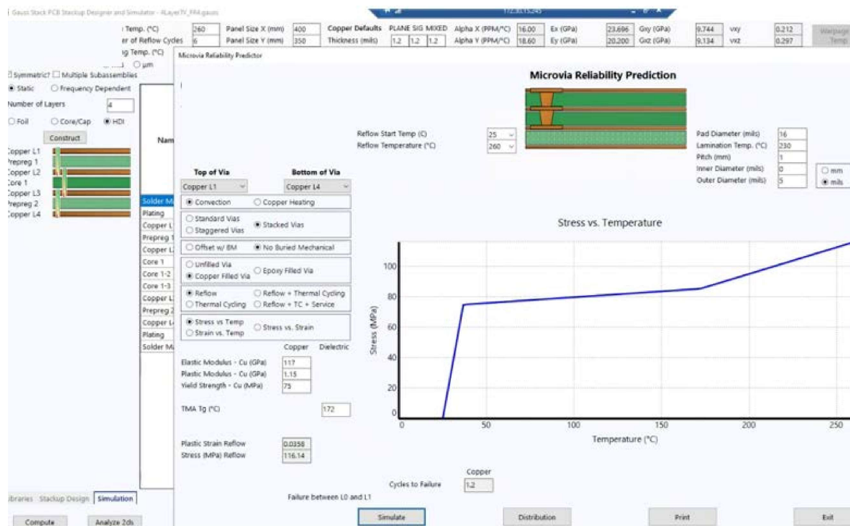


Figure 6 Simulation of solder reflow to 260°C using 100% FR-4 epoxy as the dielectric material modeling layers 1-4

Figure 7 shows the stack-up of the hybrid construction used for the stress simulations. Figures 8 – 10 summarize the stress modeling for the hybrid construction where 47 mil FR-4 epoxy is used in the subassembly and 5 mil of the unreinforced build-up material are used on the top and bottom of the PWB with no offset to the subassembly (stacked configuration). When the microvia is simulated by itself, layers 1-2, the microvia is predicted to survive > 24 thermocycles (Figure 8). When the simulation is done on all four layers, the simulation suggests that the coupons will only pass 2.4 thermocycles. This results by itself suggest that the microvias should survive reflow and likely predicts that the failure mechanism will be within the subassembly. The modeling software should be viewed as something that can be used to calculate relative stress but should not be viewed as capable of calculating absolute stress levels as there are various mechanical properties that change with temperature that are not captured.

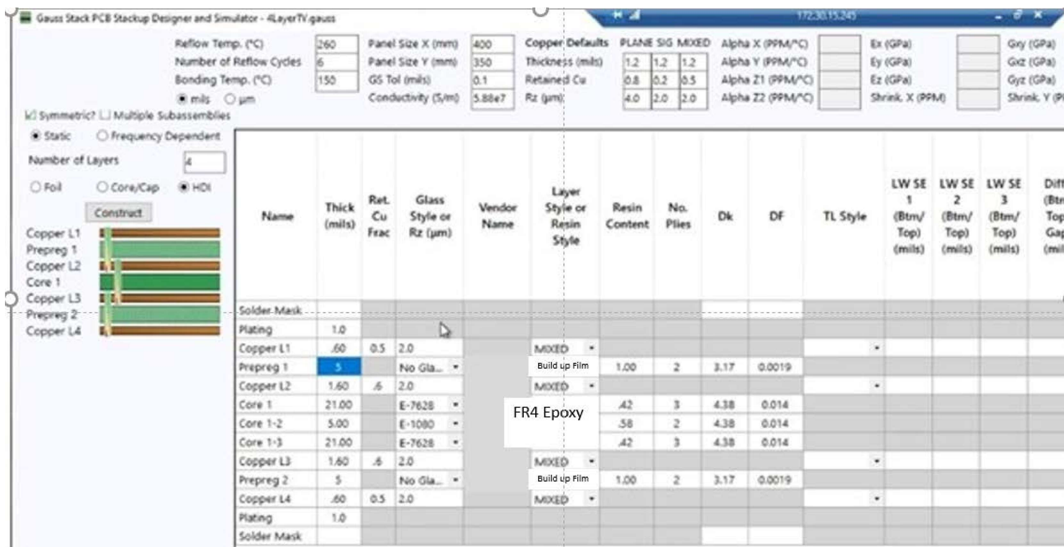


Figure 7 Hybrid Stack-up used in Simulation for 260°C thermal reflow

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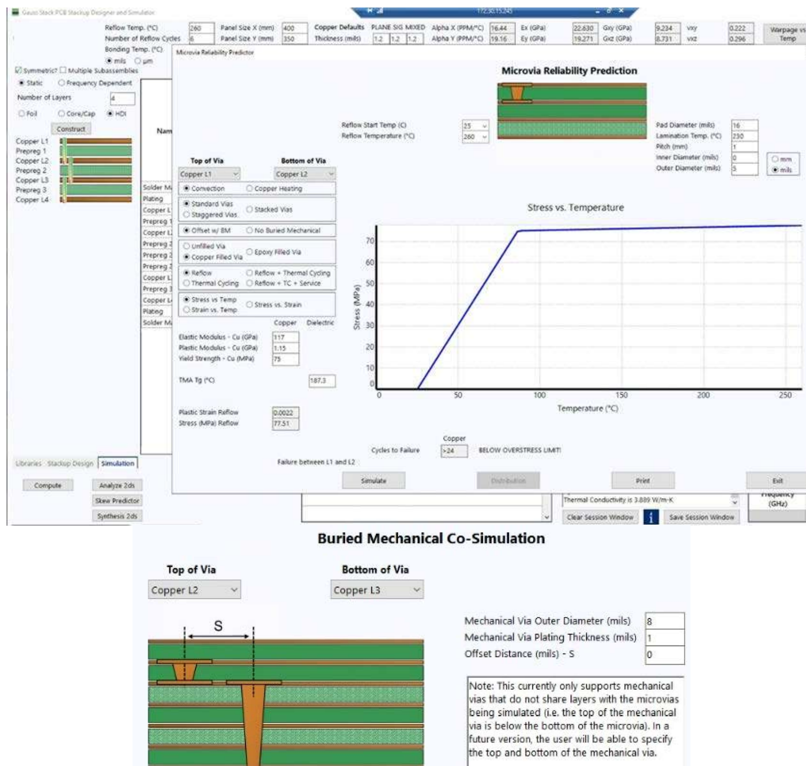

Figure 8 Hybrid Stack-up used in Simulation for 260°C thermal reflows modeling only the thermal reliability of microvia layers 1-2

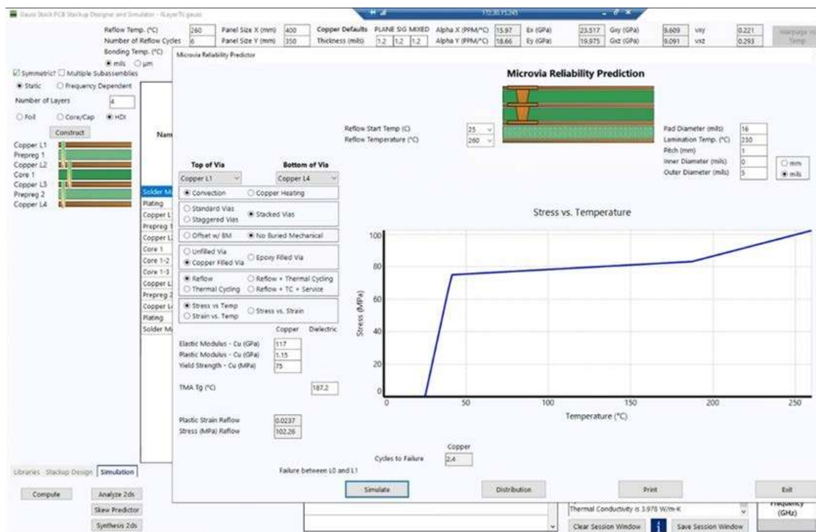

Figure 9 Hybrid Stack-up used in Simulation for 260°C thermal reflows modeling layers 1-4

Thermal Cycling Performance of the Hybrid Stack-up

Current Induced Thermal Cycling (CITC)

The CITC coupon and stack-up is shown in an earlier section. CITC coupons from 4 different fabricators were manufactured and thermally cycled under the same conditions. It needs to be emphasized that this coupon is designed to cause failure. Failure is the expectation. The goal is to push the materials to the limits to observe the weakest mechanical link. A good failure is when something around the microvia fails but the microvia itself and its attachment to the capture pad are still in place and robust. From the perspective of the materials designer, the goal is that the coupon fails by a crack in the subassembly or some type of corner crack in the attachment of the microvia to the subassembly but not within the microvia/capture pad interconnect itself. The goal is to make the microvia stronger and more robust than the subassembly. If the dielectric material is not robust and has too much X/Y/Z axis expansion, the microvia will fail somewhere at an interface related to the many manufacturing steps to create the microvia. The failure of the microvia may or may not be accompanied by cracks in the dielectric material itself. There can be many types of defects in the manufacturing of a PWB containing microvias. These include: cap plating that is

too thin as a result of planarization that is too aggressive, too much electroless copper yielding a thick weak Pd layer, oxidation of the electroless copper layer, oxidation of the flash plating layer, a copper grain structure that has very small grain size where a clear palladium layer can be seen, voids in the microvia copper via fill, deposition of organic debris at the base of the copper capture pad, incomplete removal and cleanup of the dielectric after lasing ablation, etc. The best case is epitaxial growth of the electroless copper between the capture pad copper and the copper via fill such that the electroless copper plating is invisible. This coupon tests the ability of a fabricator to create a defect free microvia. If the microvia has poor via formation for any of these reasons, failure will occur here. If microvia formation is done well and consistent, it pushes the eventual failure of the coupon to somewhere else such as a barrel crack in the subassembly or a corner crack between the subassembly and the microvia where the microvia is intact. A good failure is where microvia formation is more robust and stronger than the rest of the circuit board or when the FR-4 epoxy used to manufacture the coupon approaches decomposition before any microvia failure. This coupon is designed with an epoxy via fill in the subassembly such that there will be a lot of Z axis stress on the microvia interconnect.

The criterion for a CITC failure is when after a given thermocycle, the new ambient resistance exceeds the starting ambient resistance by 10%. A second criterion is when the ambient resistance of a given cycle exceeds the ambient resistance of a prior cycle. The third criterion is when the peak resistance of a given thermocycle exceeds the peak resistance of the previous cycle. With each successive thermocycle there will be a return to ambient resistance and a peak resistance at the highest temperature. A failure is when the following cycle peak resistance exceeds the previous cycle peak resistance by 5% or the return to ambient resistance exceeds the starting ambience resistance by 5%. The CITC coupon introduces the concept of the TCR or the temperature coefficient of resistance. This can be calculated from $R(T)-R_0/R_0$. By monitoring the TCR, a sudden change in slope at a given temperature will indicate a failure and a likely crack. The CITC performance of the four fabricators is shown in Figure 10. The CITC thermocycling suggests that fabricator 1 had a very wide distribution of performance with no infant mortality defects (failures at the 1st or 2nd thermocycle suggesting a possible fab defect). The wide breadth of performance does suggest however a lack of consistency in fabrication. Fabricator 2 showed a very narrow range of performance with all coupons failing between 22 – 28 cycles. Fabricator 3 showed 25 coupons that survived 50 cycles of thermocycling at 260°C. There were some lower performing coupons but overall, an extreme high level of performance was observed. Fabricator 4 showed some extremely good performance with the majority of coupons surviving from 32-48 thermocycles at 260°C. Fabricator 4 had some early infant mortality defects suggesting a defect in the fabrication.

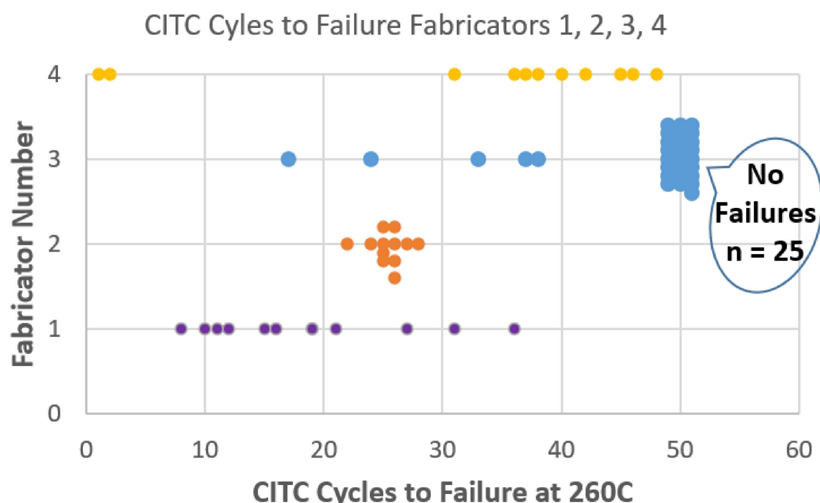

Figure 10 CITC Cycles to failure for the hybrid stack-up built by 4 fabricators

D-Coupon Testing

Similar trends can be seen in the D-coupon testing. In D-coupon testing according to IPC-TM-650-2.6.27 the peak resistance is recorded after the first reflow cycle. In successive testing, failure is reached when a particular reflow shows a peak resistance greater than 5% more than the initial peak resistance reflow. The data for Fabricators 1-4 are shown in Figure 11. D-coupon testing is noteworthy from the CITC coupon in that overall, the cycles to failure seem to be lower in D-coupon testing than CITC testing. Fabricator 4 had a narrow distribution of performance with the CITC testing including a couple infant mortality defects but the D-coupon testing seemed to expose 3 different failure mechanisms. The differences in the D-coupon layout vs the CITC layout were minor. Both had microvias separated by 1 mm pitch. The microvia diameters were the same. The observed time between reflow cycles for the D-coupons was about 6.66 minutes for the full cycle of heat up and cool down, equally split between heating up and cooling down. CITC has a similar heat up and cool down but uses a 30-40 second hold at reflow. It should be noted that for 3 out of the 4 fabricators, the D-coupons failures occurred at less thermocycles than the CITC company. The lone exception was fabricator 3. Fabricator 3 asked for an exception to the coupon design because they struggled to produce

the PWBs without excessive microvia copper voiding. Fabricator 3 built the PWBs at an aspect ratio they had confidence they could successfully plate the microvia holes shut without voids. Fabricator 3 built the microvias with a much larger 9.4–9.6 mil via (aspect ratio – 0.5). D-coupon testing and CITC testing were fairly similar for Fabricator 3 with the D-coupons actually outperforming the CITC coupons possibly suggesting a much high level of robustness of the much larger via size that was less sensitive to any testing differences between the two methods.

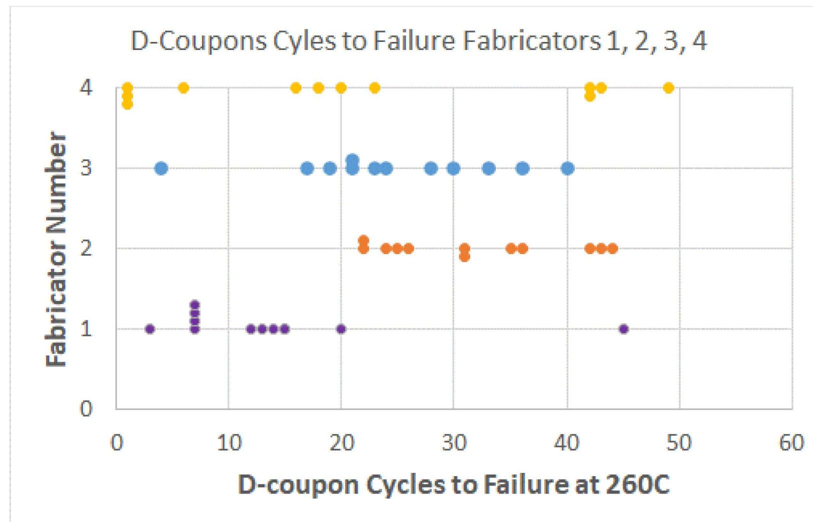

Figure 11 D-Coupon Test - Cycles to failure for the hybrid stack-up built by 4 fabricators

Failure Analysis after CITC-P/D-coupon testing

Fabricator 1

Fabricator 1 built the coupons to specification. The aspect ratio achieved was 1.01 to 1.03. Cross-sections of the unstressed condition can be seen in Figure 12. Noted defects were incomplete plating of the microvias with voided areas within the microvia. Figure 13 shows the microvia dimensions at the top and bottom of the coupons. Figure 14 shows SEM images at 900X showing the top and bottom microvia copper plating. There is no epitaxial plating across the boundary layers of the cap plating to the filled copper of the microvia. Two very different copper crystal structures can be observed between the cap plating of the subassembly and the microvia plating. Figure 15 shows a cross section of the coupon that failed after 10 D-coupon thermocycles. It should be noted that in the D-coupon testing, all coupons were stressed to 48 cycles of 260°C thermocycling regardless of whether or not they failed at one cycle or 48 cycles. Therefore, the failures should be expected to be more pronounced. A coupon that failed after 10 cycles and then is thermocycled an additional 38 cycles would be expected to show a more exaggerated defect. Figure 14 shows a fairly dramatic separation at the cap plating to microvia interface.

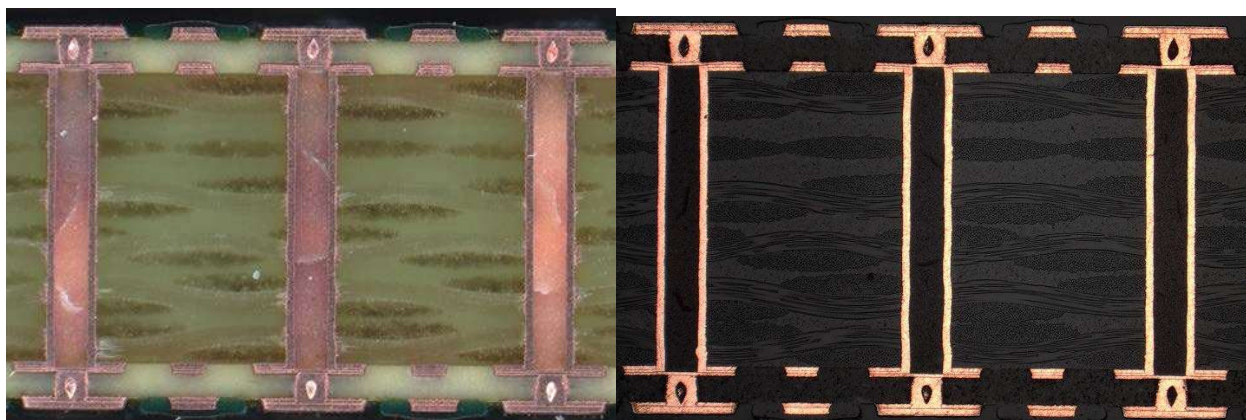

Figure 12 Cross-sections of the hybrid stack-up built by Fabricator 1 as manufactured prior to any thermocycling

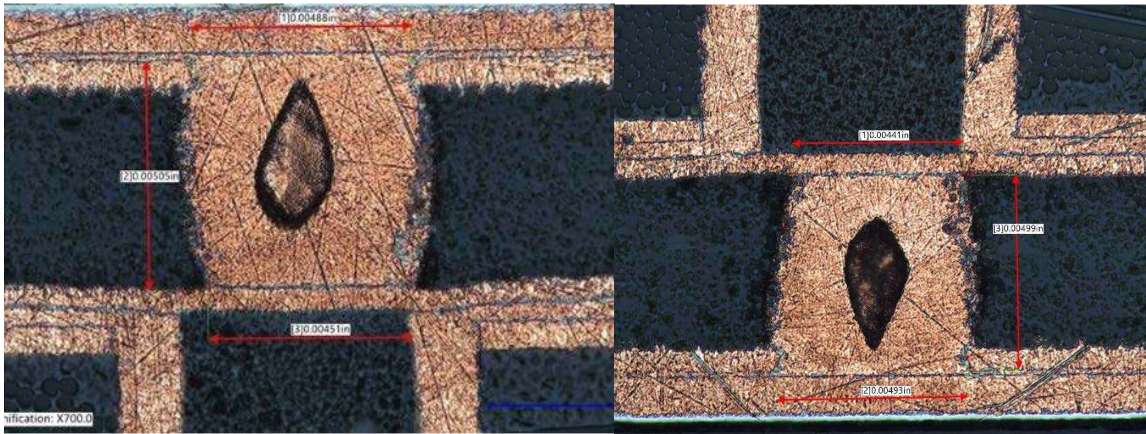

Figure 13 Cross-sections of the top and bottom microvias from the hybrid stack-up built by fabricator 1 as manufactured prior to any thermocycling showing an aspect ratio of 1.01 to 1.03.

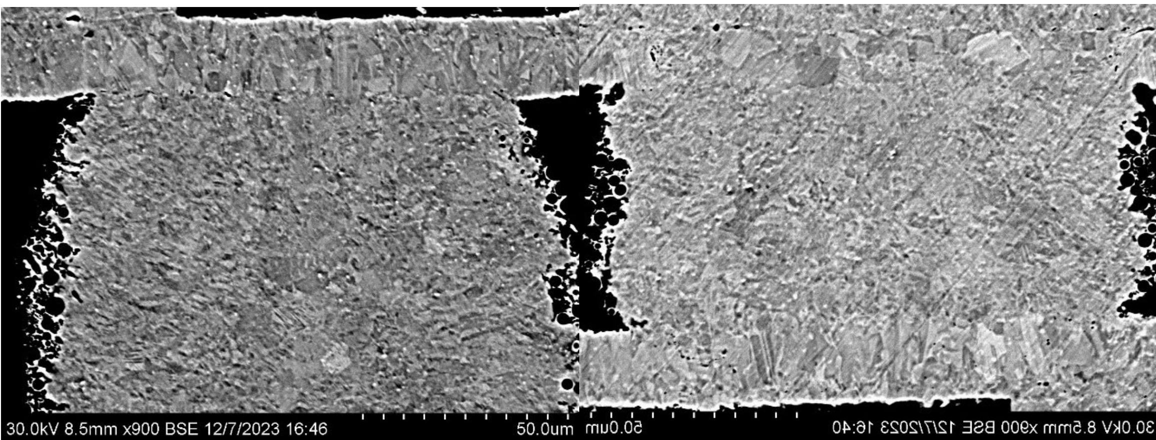

Figure 14 SEM images of the top and bottom microvias from the hybrid stack-up built by Fabricator 1 as manufactured prior to any thermocycling showing a very different crystal structure between the microvia plated copper and the cap plating copper (900X magnification).

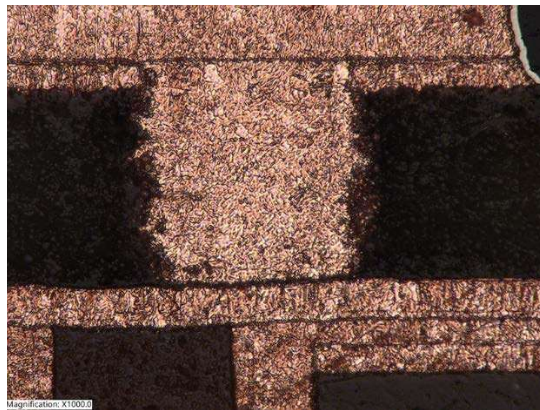

Figure 15 Cross-section of the top microvia from the top built by fabricator 1 that failed after 10 D-coupon thermal cycles suggesting a failure at the electroless copper to cap plating interface.

Fabricator 2

As noted above Fabricator 2 requested an exception to the coupon design due to difficulty fabricating the PWBs. Fabricator 2 built the coupons using a microvia dimension they were confident they could achieve good microvia plating/filling. Figure 16 shows cross-sections of the coupons in the unstressed condition. Figure 17 shows cross-sections at higher magnification showing the microvias to have an aspect ratio of approximately 0.5. Figure 18 shows SEM images at 250X and 2000X showing what looks to be epitaxial copper growth from the cap plating to the microvia plated copper. There appears to be one consistent copper structure across the boundary area. The SEM images do capture some cracks in samples that have not yet been exposed to D-or CITC thermocycles. Figure 19 shows cross-sections of a D-coupon failure after 22 thermocycles. Amongst the

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4 fabricators, only this failure mode was observed in coupons built by Fabricator 2. The coupons show extreme surface deformation and were the only coupons to show this extreme level of surface deformation. The areas top and bottom between the microvias seems to be in a permanent state of expansion. The microvia areas themselves show less permanent Z axis expansion as they probably acted as rivets holding the pwb together. Figure 18 shows the failure of these coupons at higher magnification. The stress level must have been very high for cracking to occur at the interconnect between the microvia joint and the connecting copper signal trace between the daisy chain microvias. Figure 17 shows this cracking occurring at the same junctures in many locations at the surface of the coupon between the microvias and the connecting trace. This suggests that the microvia itself and the microvia connection to the capture pad is extremely robust such that failure occurs in areas outside of the microvia that one does not typically observe with microvia failures.

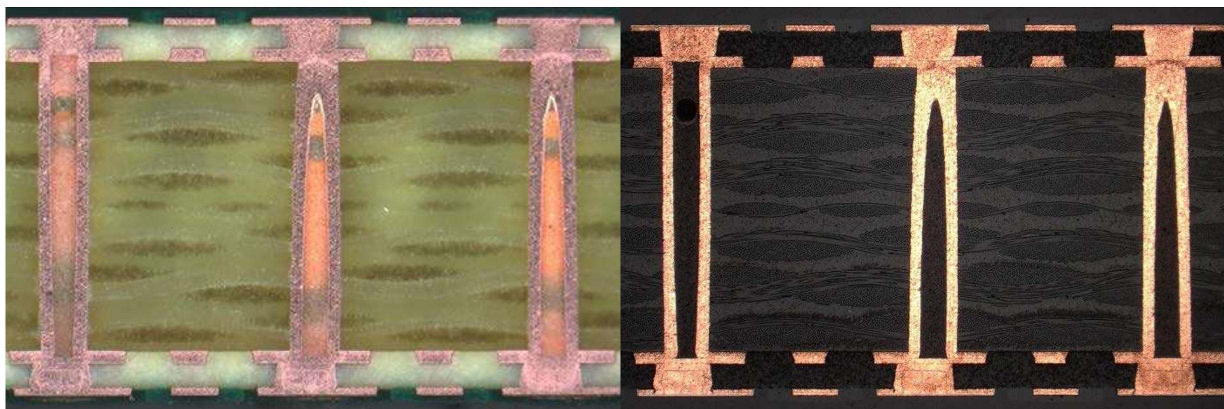

Figure 16 Cross-sections of the hybrid stack-up built by fabricator 2 as manufactured prior to any thermocycling (note the larger microvia size)

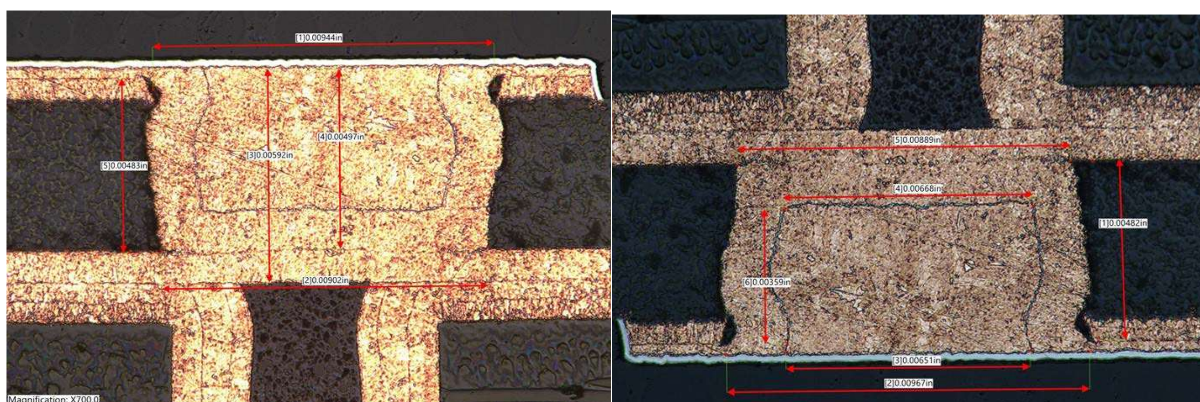

Figure 17 Cross-sections of the top and bottom microvias from the hybrid stack-up built by fabricator 2 as manufactured prior to any thermocycling showing an aspect ratio of ≈ 0.50.

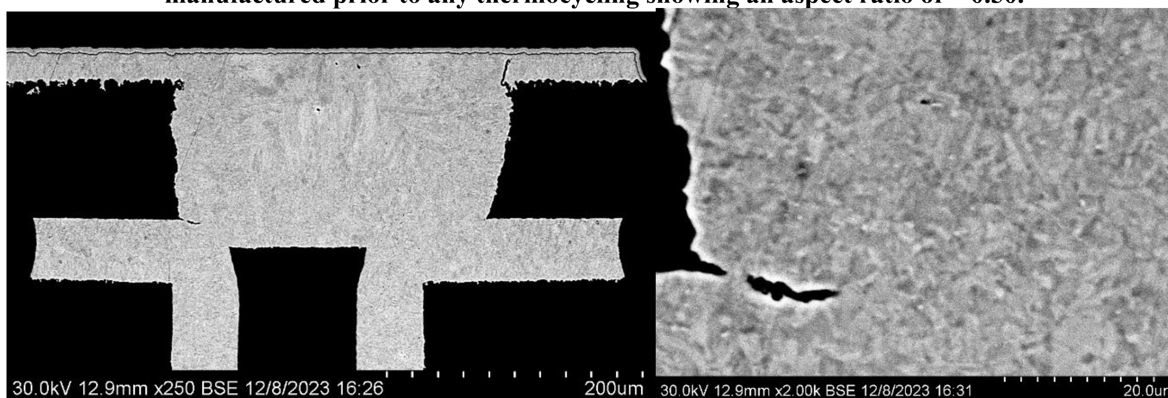

Figure 18 SEM images of the top microvia from the hybrid stack-up built by Fabricator 2 as manufactured prior to any thermocycling showing a consistent crystal structure between the microvia plated copper and the cap plating copper (left 250X, right 2000X magnification). Note the presence of cracks.

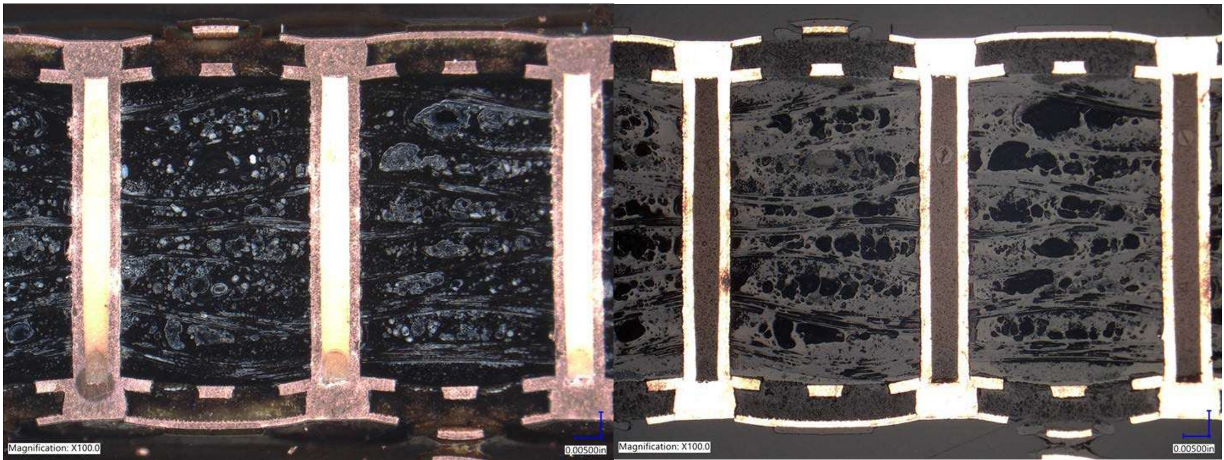

Figure 19 Cross-section of the hydrid stack-up from fabricator 2 that failed after 22 D-coupons thermal cycles suggesting a crack in the surface copper interconnecting the daisy chain of microvias.

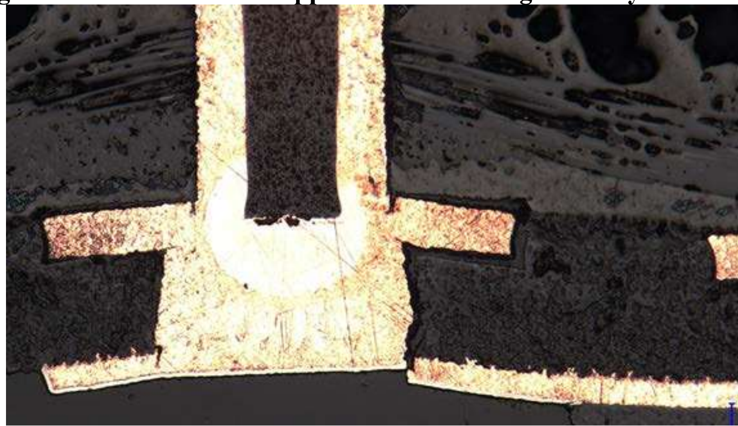

Figure 20 Higher magnification cross-section of the hydrid stack-up from fabricator 2 that failed after 22 D-coupons thermal cycles suggesting a crack in the surface copper interconnecting the daisy chain of microvias.

Fabricator 3

Fabricator 3 built the pwbs to print with good quality. Cross-sections of the as manufactured coupons are shown in Figure 21. Figure 22 shows cross-sectional images of the top and bottom microvias with an aspect ratio 0.93-0.99.

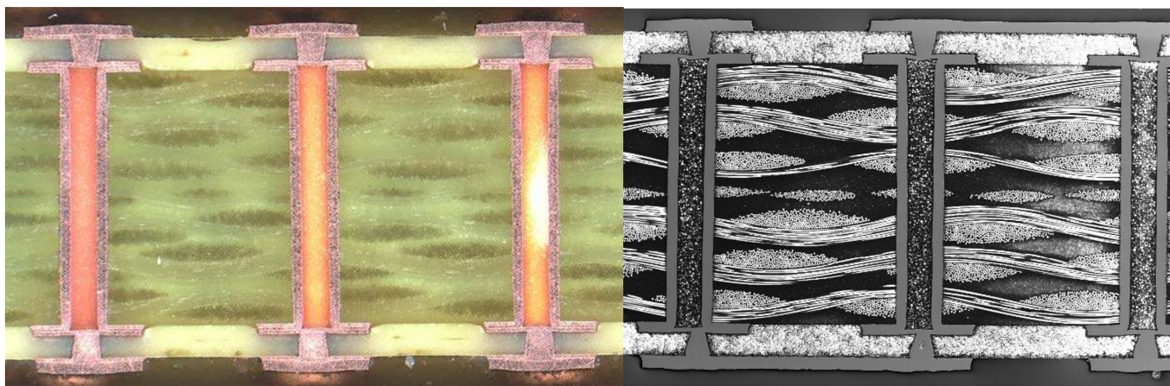

Figure 21 Cross-sections of the hybrid stack-up built by fabricator 3 as manufactured prior to any thermocycling (optical micrograph left, SEM 50x right)

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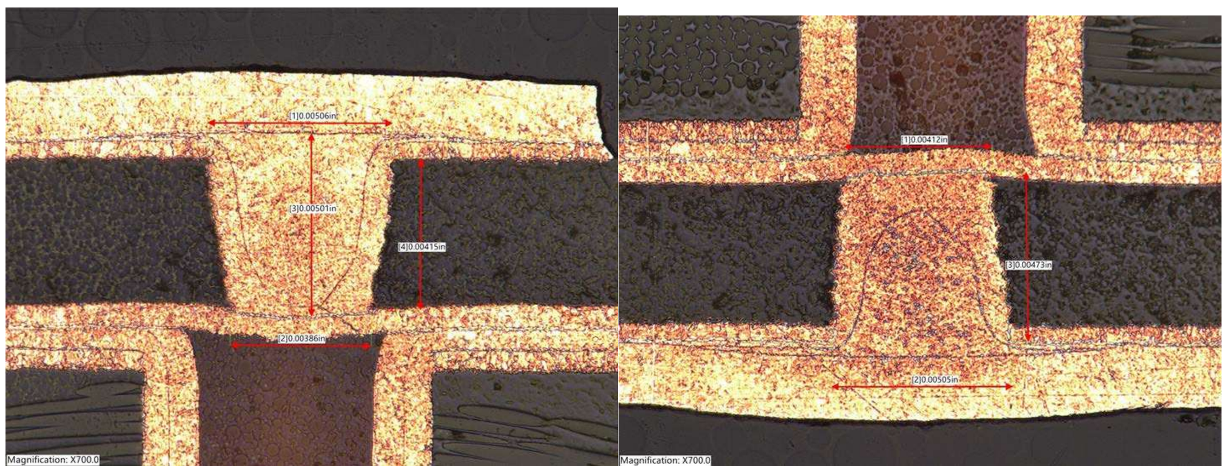

Figure 22 Cross-sections of the top and bottom microvias from the hybrid stack-up built by fabricator 3 as manufactured prior to any thermocycling showing an aspect ratio from 0.93 to 0.99.

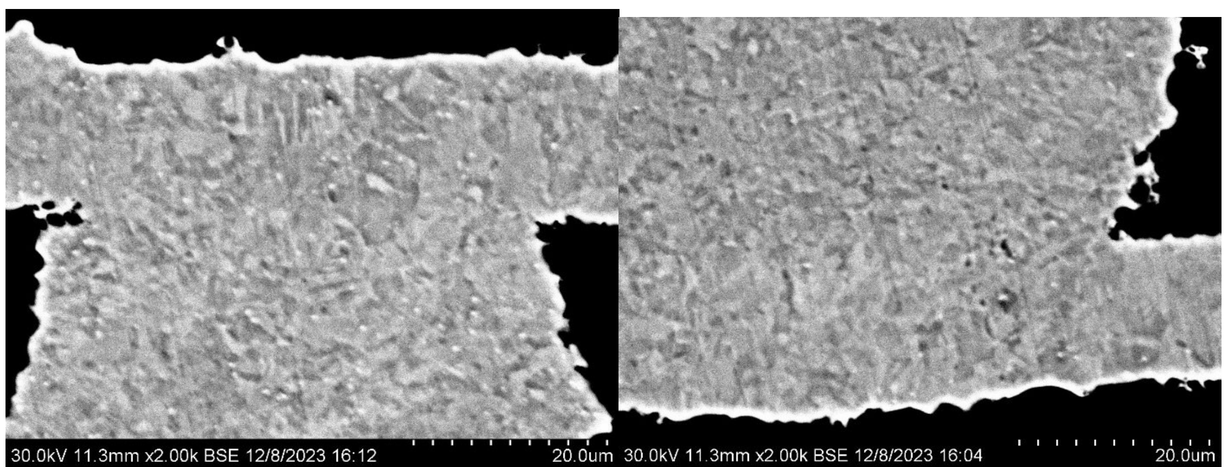

Figure 23 SEM images (left, right x2000X) showing what appears to be epitaxial crystal growth between the cap plating layer and the microvia copper plating.

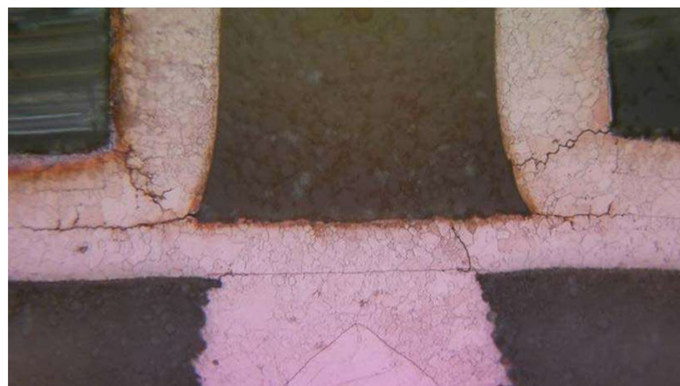

Figure 24 Cross-section of the bottom microvia built by fabricator 3 that failed after 17 CITC (260◦C) thermal cycles suggesting corner cracks at the bottom of the epoxy filled mechanical drilled subassembly.

Figure 25 Cross-section of the hybrid stack-up built by fabricator 3 that failed after 17 D-coupon (260°C) thermal cycles suggesting severe barrel cracks in the subassembly, corner cracks at the top and bottoms of the wrap plating, as well as microvia separation from the cap plating.

The SEM images of Figure 23 show uniform copper growth in the microvia plating on top of the cap plating copper. The desired epitaxial copper growth appears to be achieved with a uniform copper crystal structure at the interface. As shown in Figure 24, after 17 CITC-P thermocycles there were clear barrel cracks near the juncture of the mechanically drilled subassembly to the microvia. Because there was interest in obtaining 48 thermocycles with the D-coupon testing to see how long the best coupons could survive and all coupons remained in the oven regardless of when they failed, a failed coupon that could fail at 20 cycles would still experience 28 more thermocycles of stress such that the failure/deformation should be or could be significantly greater than if one were to pull the failed coupon immediately out of the oven immediately after failure. Figure 25 appears to be indicative of a lot of extra stress being applied to the coupon after the initial failure. Figure 25 is not ideal because the micro sectioning occurred at the back of the microvia hole, but the image is still revealing. There are a lot of cracks in the subassembly and there are a lot of cracks at the juncture/corner of the subassembly barrel/foil copper. In areas where the foil copper and cap plating is intact, sections of the plated mechanically drilled subassembly have broken off. We have evidence from the CITC failure analysis that the subassembly barrels are cracking before without any evidence of microvia cracks. This suggests that the mechanism is more likely than not that cracks form in the subassembly copper plating after some number of D-coupon 260°C thermocycles, after which there is still an enormous amount of stress caused by the expanding and contracting FR4/via fill such that damage occurs to the microvia.

Fabricator 4

Fabricator 4 asked for an exemption from the design print replacing some layers of FR4 epoxy. It was thought that the fabricator would replace the FR4 epoxy layers with another vendor of FR4 and not use sheets of the unreinforced bonding material. There will be less stress created by the subassembly because the presence of the unreinforced material reduces the overall Z axis expansion of the subassembly. For this reason, extremely high levels of performance should be taken with a note of caution because the overall stress levels will be less than the coupons built by Fabricators 1 and 3. Figure 26 shows the ability of the fabricator to plate the middle of a deep mechanically drilled hole. However, the epoxy via fill is less than perfect as there is not complete epoxy via filling. Cap plating extends down into the mechanically drilled subassembly. This was expected to be a source of thermocycling failure but it was not detected in this study.

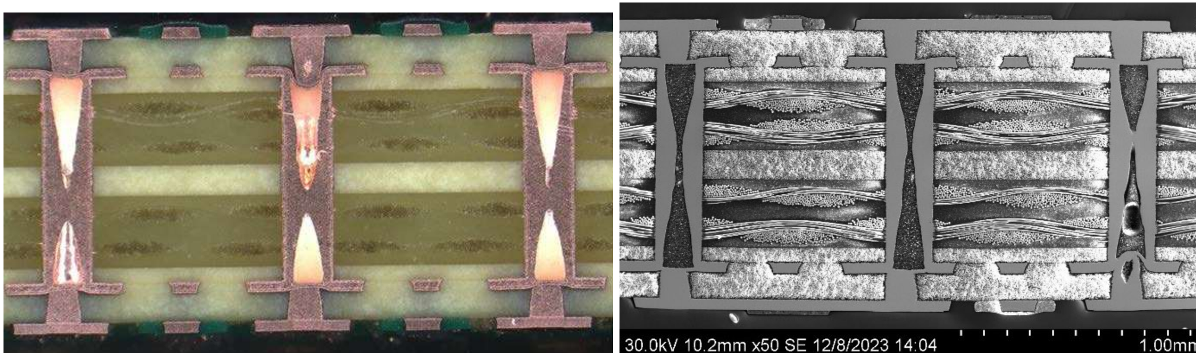

Figure 26 Cross-sections of the hybrid stack-up built by fabricator 4 as manufactured prior to any thermocycling (optical micrograph left, SEM image x 50X)

Figure 27 shows the aspect ratio of 0.94 to 1.01 achieved by Fabricator 4. Figure 28 shows SEM images at 250X and 900X respectively. While the cap plating and microvia copper plating appear highly crystalline and not amorphous, there does not appear to be epitaxial copper growth across the interface boundary region suggesting the best possible interconnect. Figure 29 shows a fairly easy to find infant mortality defect after one D-coupon thermocycle using only optical microscopty. It needs to be emphasized that the D-coupons were exposed to 48 260°C thermocycles. Even if they failed after one cycle the crack itself should or could be more pronounced and easier to find. Figure 30 shows other views using the optical microscope where there is obvious separation and there appears to be an anomoly in the electroless copper layer.

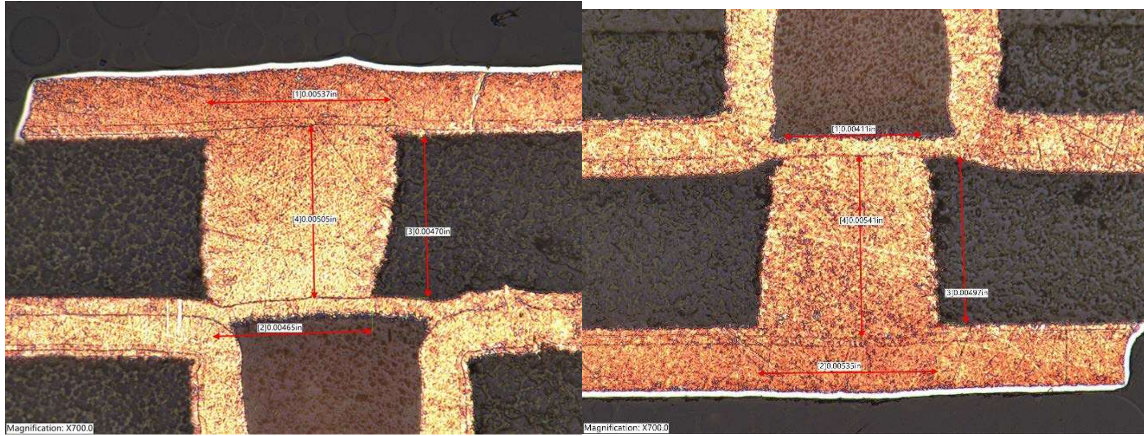

Figure 27 Cross-sections of the top and bottom microvias from the hybrid stack-up built by fabricator 4 as manufactured prior to any thermocycling showing an aspect ratio from 0.94 to 1.01.

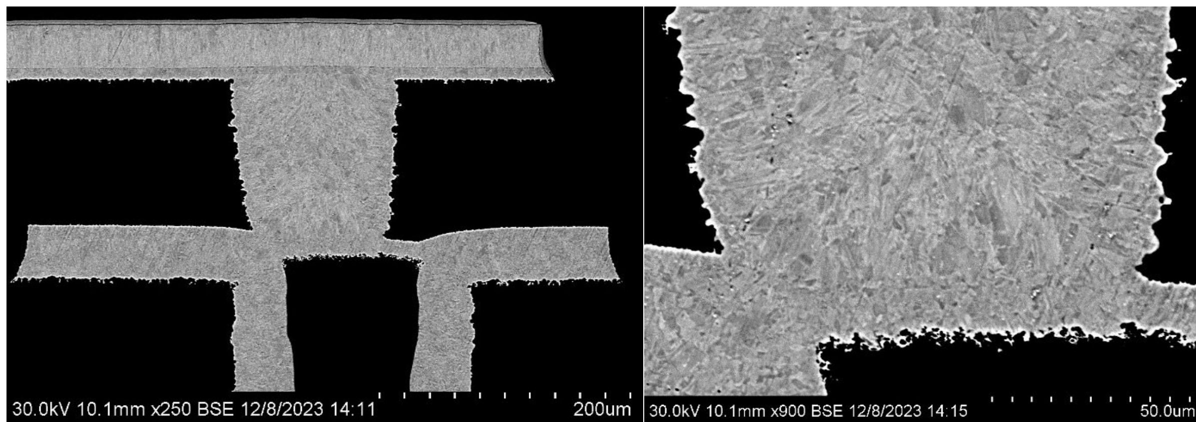

Figure 28 SEM Images (250X left, 900X right) showing two different plating coppers in the cap plating layer and the microvia plating layer. There does not appear to be epitaxial copper growth at the interface.

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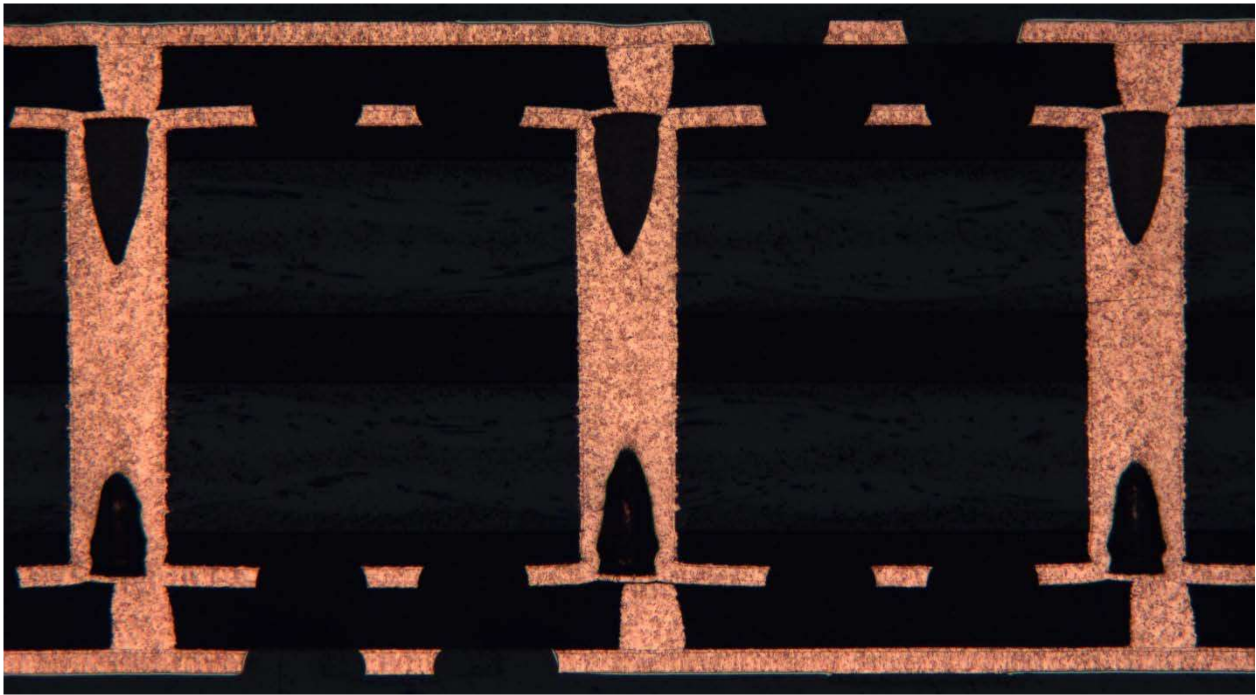

Figure 29 Cross-section of the hybrid stack-up by fabricator 4 that failed after 1 D-coupon (260◦C) thermal cycles suggesting a weak copper interface between the capture pad and the microvia.

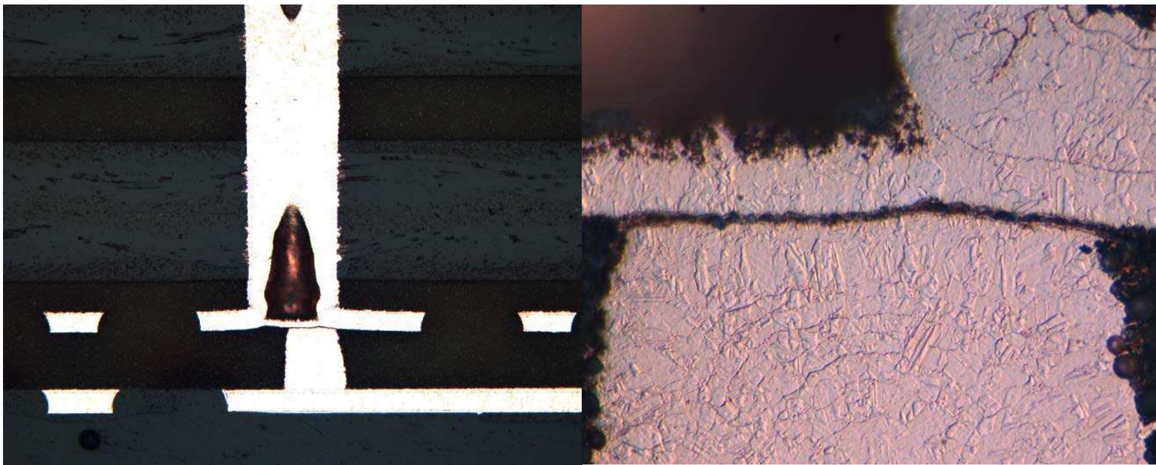

Figure 30 Cross-sections of the hydrid stack-up by fabricator 4 that failed after 1 D-coupon (260°C) thermal cycle suggesting a weak copper interface between the capture pad and the microvia.

Focused Ion Beam (FIB) analysis was carried out by a 3rd Party outside lab to further characterize the microvia to capture pad separation shown in Figure 30. The images in Figure 31 shows the microvia and boundary area prior to FIB ablation. Figure 31 suggests that there are two distinct passes of electroless copper, and that the failure takes place between the electroless layers. Figure 32 shows high magnification (12000x) images of the failure region between what appears to be two distinct layers of electroless copper suggesting the fabricator did two electroless passes and failure occurred between two separate electroless copper depositions. Figure 33 is an image showing the interface failure in 3 dimensions. For comparative purposes, Figures 34 (a-c) is included which shows classic microvia failures provided by the same third-party expert lab that does independent microvia failure analysis routinely. Figure 34a shows a classic "weak" microvia boundary area. Figure 34b shows a classic failure of the electroless copper to the copper microvia via fill. Figure 34c shows a classic failure at the electroless copper layer where the electroless copper delaminates or debonds between the microvia electroplating layer and the cap plating layer, failing above and below the electroless copper layer and little to no electroless can be seen in various areas. Figures 34(a-c) are included as instructional to provide insight into why it is believed that Fabricator 4 performed two electroless copper plating depositions and that the early infant mortality failures occurred between two electroless copper depositions. Figure 35 shows an unusual failure at the joint of the microvia to cap plating layer. The Figure 35 joint failure is unusual as it suggests that when the microvia is not aligned well over the subassembly, some higher-level stress state must be attained. This

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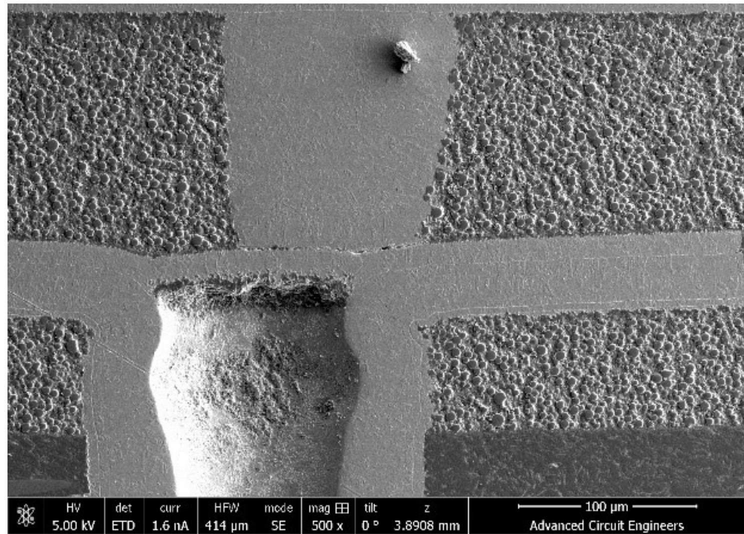
suggests that when comparing stacked microvias to staggered microvias, registration is still critical in the stacked configuration so as to not create unbalanced stresses at the base of the microvia.



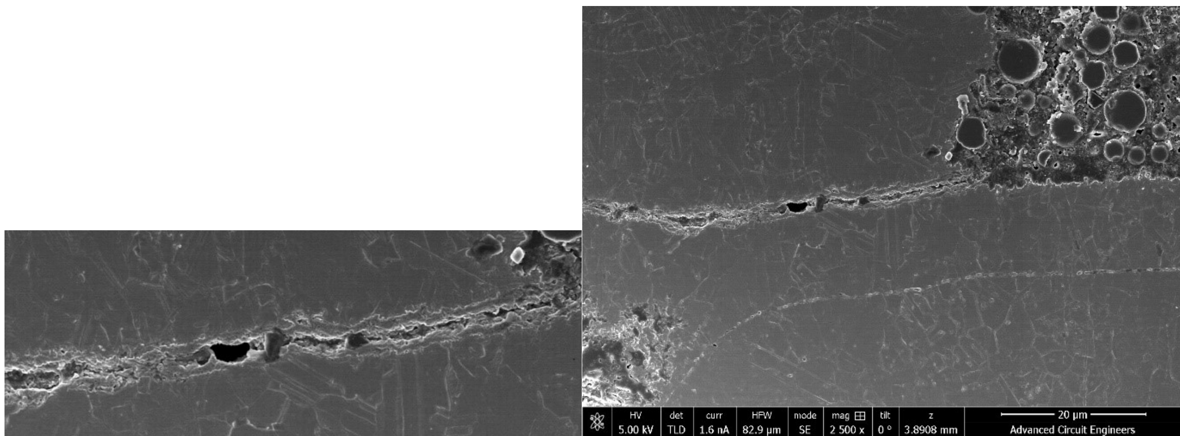


Figure 31 Fabricator 4 coupon which failed after 1 D-coupon cycle prior to FIB ablation suggesting a separation between two distinctive electroless copper treatments

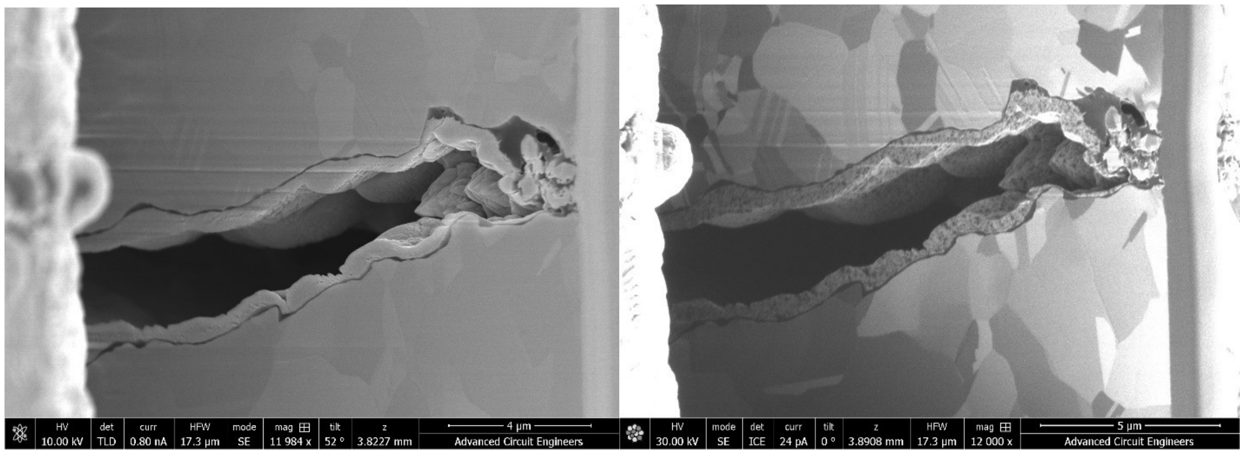


Figure 32 Fabricator 4 coupon which failed after 1 D-coupon cycle prior to FIB ablation suggesting a separation between two distinctive electroless copper treatments (12000x)

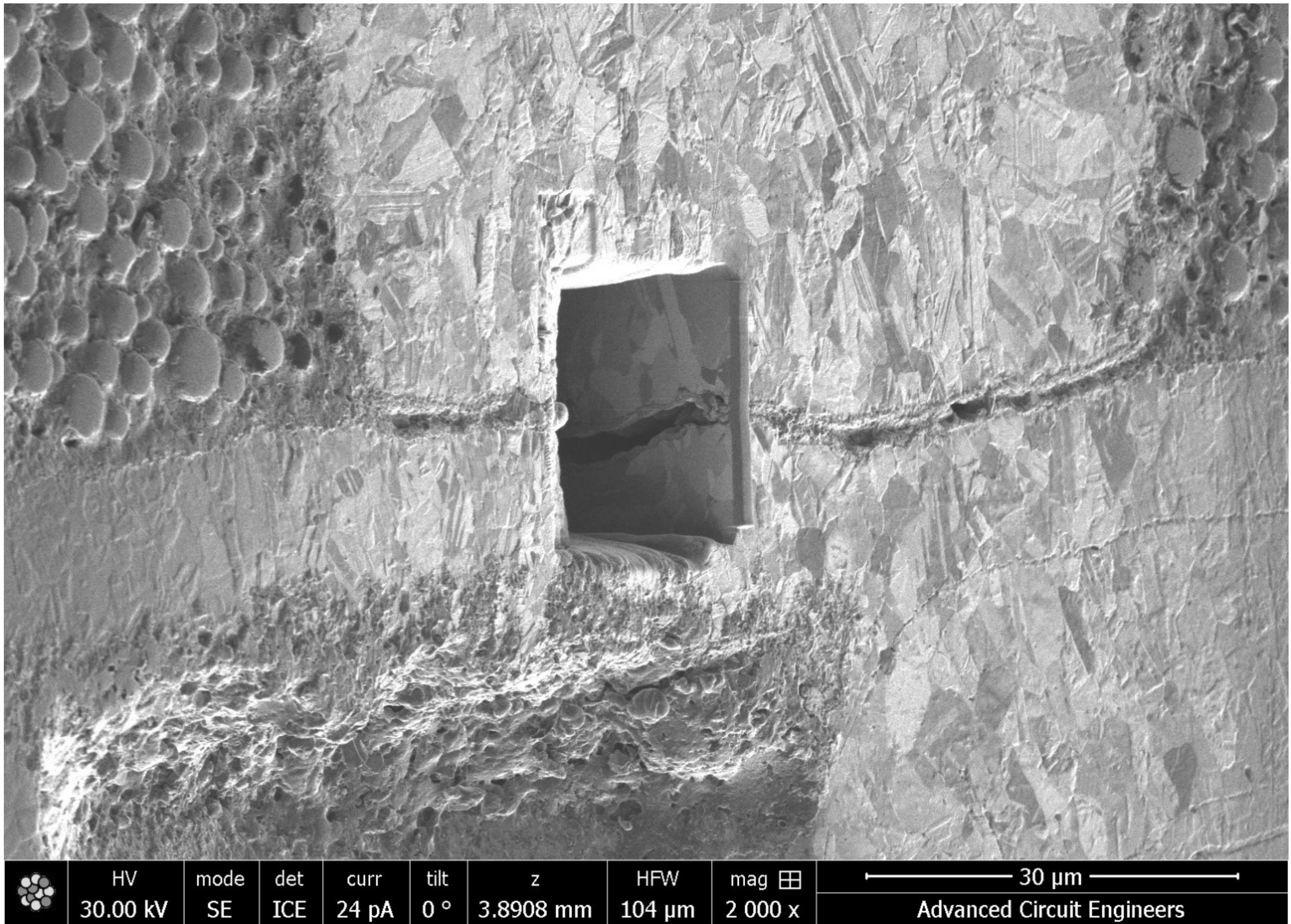


Figure 33 Fabricator 4 coupon which failed after 1 D-coupon cycle prior to FIB ablation suggesting a separation between two distinctive electroless copper treatments

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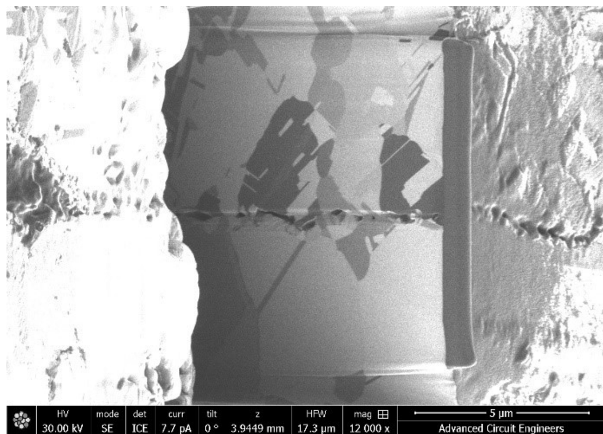
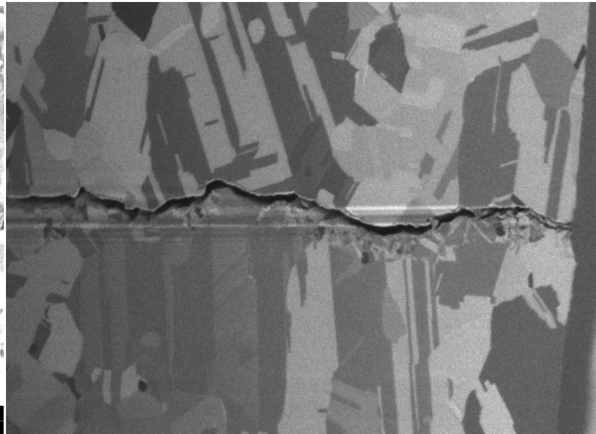
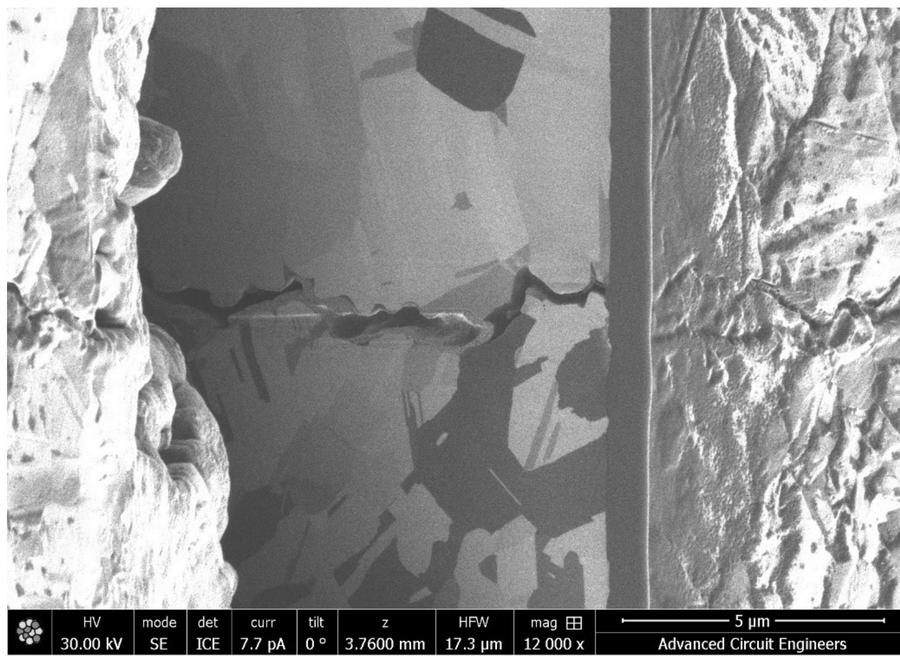


(34a)



(34b)



(34c)

Figure 34(a-c) show FIB images supplied from an independent expert microvia failure analysis lab. (a) a typical "weak" microvia (b) a classic electroless copper failure to one of the boundary layers to the copper via plating and (c) a delamination of the electroless copper to both the cap plating and the plated copper of the microvia

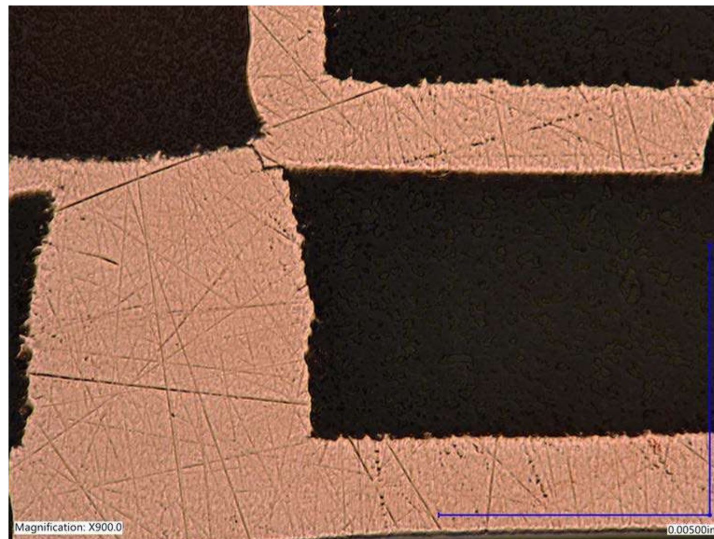
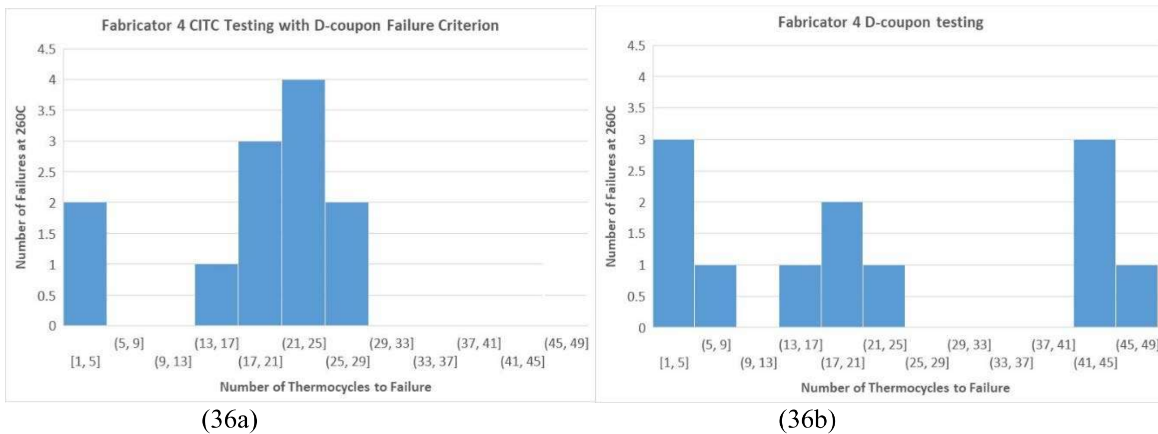


Figure 35 Cross-section of the hybrid stack-up by fabricator 4 that failed after 2 D-coupon (260°C) thermal cycles suggesting a weak interface in the cap plating layer.

Discussion

There is some variation in the results between the D-coupon testing (IPC-TM-650 TM-2.6.27A) and the CITC coupon testing (IPC-TM-650-2.6.26B). The two methods differ in their failure criterion. D-coupons results are based on a 5% increase in resistance from the peak resistance of the first thermocycle. CITC testing is an adaptive test where a failure is a result of more than a 5% change in peak resistance between cycles and an overall 10% increase in resistance from the initial cold resistance. CITC testing has a 30-40 second interval at the peak temperature whereas D-coupon testing is a simple peak at 260◦C. D-coupon testing depends on the change in bulk resistance from the second reflow cycle onward. Partial cracks may show up as a >5% resistance change at any given thermocycle. CITC testing relies mostly on the changing resistance from thermocycle to thermocycle and a failure is a 5% change between thermocycles. CITC testing will show the instantaneous complete crack. It is not the goal of this publication to pass judgement on different IPC test methods. Both methods provide valuable insights into the mechanisms of PWB, via, or microvia failure. Figure 36a shows the CITC results for Fabricator 4 when evaluated according to the D-coupon criterion and Figure 36b shows the actual D-coupon results. The results are fairly similar in that there is an infant mortality population at 1-2 cycles and there is a distribution of failure around 13-29 cycles. Fabricator 4 does have a few data points approaching 50 thermocycles when using the D-coupon criteria.

Regardless of the failure criterion, expert failure analysis is necessary to determine the root cause of failure, the extent of any cracking and to differentiate between just an increasing bulk resistance and crack propagation. Figures 5-7 predict that pure FR4 epoxy will only survive one thermocycle in this test vehicle, 5-10 cycles if you only model the microvia layers 1-2. Therefore, for FR4, one would not be expected to see more than a few thermocycles at 260◦C. Figure 8 shows that when the nonreinforced material is used to form the microvia layers, when the subassembly is comprised of FR4 type epoxy, the microvia layers 1-2 and 3-4 would be expected to survive > 24 cycles using the simulation software. Figure 9 shows that when the nonreinforced material combined with the FR4 epoxy subassembly is modeled through all layers 1-4, the complete D/CITC coupons would be expected to survive only 2.4 cycles using the simulation software. The modeling software is less than perfect but one can make the argument that this test coupon design is effective in creating a high enough stress level to cause a microvia to fail. When the microvia is more robust than the rest of the coupon, the modeling software predicts that the coupon will fall apart around the microvia. Indeed, this is what happens. Fabricator 1 did not have any obvious infant mortality defects. D/CITC coupon testing suggested an average survival rate of 16/19 cycles respectively. Cross-sectioning of the failures were consistent showing a cap plating to microvia/electroless layer.



(36a) (36b)

Figure 36(a,b) Figure 32a shows the thermocycling results for Fabricator 4 when the change in resistance with each cycle is evaluated using D-coupon criterion. Figure 32b shows the actual D-coupon results for comparison.

Failure.
Failure could be seen using an optical microscope without a need for further magnification. Because this failure mechanism could be readily observed with the optical microscope, further analysis was not conducted. Because much higher performance can be achieved, one can tentatively conclude that Fabricator 1 could improve its electroless copper/pad cleaning process to achieve better results. Fabricator 2 built the design with a microvia size of 9 mils and an aspect ratio of 0.5. This was an extremely robust microvia. Severe stress deformation occurred at the surface in order to cause the surface trace copper to fully crack between microvias. It should be noted that "cracks" or "separations" were observed in unstressed coupons, so the thermal cycling seemed to add more stress to an existing defect. Fabricator 3 results are most interesting because the CITC results shows that when the PWB is properly fabricated, the microvias can be extremely robust under these high stress levels. D/CITC coupon testing suggested average survival rates of 28/43 thermocycles respectively. Failure analysis revealed cracks in the subassembly/cap plating joints. This suggests that when the microvia is properly manufactured, failure occurs somewhere else in the coupon. Fabricator 4 is interesting for other reasons as there appear to be a bimodal or trimodal distribution of failure mechanisms. Figure 26 shows a manufacturing defect where the mechanically drilled subassembly is not fully filled with epoxy via fill material. The cap plating layer extends down into the mechanically drilled subassembly through hole. It is noteworthy that no thermocycling defects could be traced to this defect. The CITC results for Fabricator 4 were robust with an average of 35 cycles when two infant mortality coupons were included in the data and 41 thermocycles when they were not included. This suggests that the microvia built with the unreinforced dielectric film can be extremely robust when the manufacturing is consistent. The D-coupon testing from Fabricator 4 averaged 26 thermocycles when all the infant mortality data points were included and 31 thermocycles when they were not included. The infant mortality failures were clearly associated with what looked to be a weak electroless copper layer where it appears the fabricator applied two electroless copper depositions and the failures from 1-2 thermocycles resulted from a clear delamination between two distinct electroless copper layers. Fabricator 4 had some coupons approach 40-50 D-coupon thermocycles, however it must be noted that Fabricator 4 substituted some of the unreinforced build-up film into the subassembly, such that the Z axis expansion of these coupons was the lowest of the 4 fabricators. This is just more evidence that if the Z axis expansion of the subassembly can be reduced in addition to using a low Z axis build-up film, a higher level of reliability should be anticipated.

Conclusion
Thick subassemblies of any material with a high Z axis expansion like FR4 epoxy can induce an incredible amount of stress on a microvia in the Z axis when the microvia is attached directly over the subassembly with no offset and the subassembly mechanically drilled via is filled with an unreinforced epoxy via fill. Figures 19 and 25 are good examples of the amount of deformation that can be created with this test vehicle. The modeling suggests that the microvia itself should be able to survive >24 thermocycles when built with this test vehicle using an unreinforced material with low Z axis CTE but the overall test vehicle would not be expected to survive more than a few thermocycles. This was partially true. In PWBs containing microvias, the weakest link is generally the foil copper/cap plating//electroless copper/microvia copper via fill interface. For the most part, these coupons showed exceptional reliability when there were no obvious manufacturing defects. The CITC testing for Fabricator 3 was exceptional and consistent showing that when the fabrication is good, an extremely high level of reliability can be obtained. D-coupon testing for Fabricator 4 was intriguing because it showed that on the one hand, coupons can be created that reach almost 50 thermocycles at 260◦C without failure. The obvious manufacturing defects or electroless copper fabrication steps can be improved/optimized to avoid the infant mortality results. One goal of this research was to show that exceptional microvia reliability can be achieved in the worst of high stress conditions. The second goal was to demonstrate that when a suitable material is used to create the microvia, the surrounding PWB will fail before the microvia layers do. A further goal was to try to suggest that when a suitable build-up material is used, the processing window can be widened such that less

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than desirable fabrication can occur and the microvia layers will still survive. This has not been achieved. The infant mortality defects suggest even when employing a unreinforced dielectric material with extremely low Z axis expansion, if the electroless copper layer at the base of the microvia is not properly manufactured and there is not a good strong interface anchoring the microvia, early failure will occur.

Acknowledgements

Special thanks to Kevin Knadle and all his expert insights into microvia reliability.
The unreinforced dielectric materials used for this study were provided by AGC Multi Material America.
Robisan Labs was contracted for all the D-coupon thermal reliability work, FIB characterization, some failure analysis, and reference material for weak microvia failure.

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