The formulating technology of extremely low loss PCB material for 112/224 Gbps without sacrificing reliability

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Abstract

We have developed an extremely low loss material that has a dielectric loss factor (Df) of less than 0.001 while simultaneously satisfying the mechanical and thermal reliability required for PCBs operating at 112 and 224Gbps. Data processing technologies such as artificial intelligence are accelerating the need for datacenters to process vast amounts of information at ever higher speeds. Therefore, further Df reduction of PCB materials is important for 112 and 224Gbps applications. In general, materials with low polarity have low Df. However, these low polarity materials typically have weaker interactions, resulting in lower mechanical and thermal reliability. Therefore, it is common to introduce polar components to meet the reliability requirements for PCB materials even at the cost of increasing Df. Because of this tradeoff, it is challenging to achieve extremely low Df in conventional PCB materials.. We have overcome this tradeoff by deriving possible solutions to improve reliability without relying on polar interactions. By applying this extremely low loss material, the signal integrity (SI) was greatly improved compared with existing low loss materials. The processability and reliability performance of the material was verified with our internal PCB, based on MRT-7. In addition to Df, lower dielectric constant (Dk) has the potential to improve SI. Therefore, for further SI improvement, we investigated how substituting filler types can lower and control Dk. It was revealed that Dk could be lowered to less than 2.6 while keeping Df < 0.001.

Introduction

PCB materials are required to have significantly lower loss for 112 and 224Gbps applications. Data processing technologies such as artificial intelligence are accelerating the need for data centers to process vast amounts of information at ever higher speeds. Therefore, further loss reduction is important for PCB materials for 112 and 224Gbps applications. Transmission loss consists of dielectric loss, conductor loss, and scattering loss. Dielectric loss = $K \times f \times \sqrt{Dk} \times Df$ (K: constant, f: frequency). As Df is proportional to dielectric loss, Df plays a large role on total loss. Df is a measurement of signal attenuation caused by electromagnetic waves being absorbed by the dielectric material. Polarization causes a phase angle, wherein the tangent of this angle is Df. Therefore, materials with low polarity theoretically have low Df [1]. However, these low polarity materials tend to have weaker interactions, resulting in lower mechanical and thermal reliability. Therefore, it is common to introduce polar components to meet reliability requirements, even at the cost of higher Df. For example, while highly polar functional groups such as epoxy and bismaleimide (BMI) work well to improve adhesion with Cu and thermal reliability through high reactivity, because they are high polarity, they usually deteriorate Df.. Due to this tradeoff, it is challenging for conventional substrate materials to achieve a low Df with robust thermal and mechanical reliability performance.

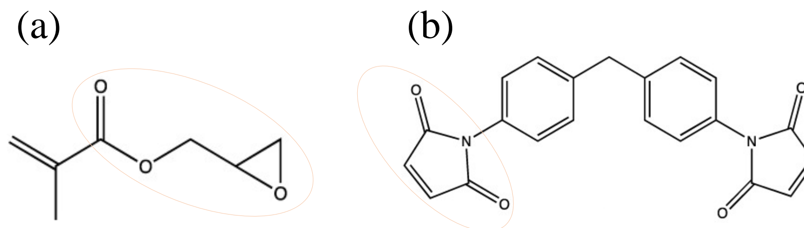


Figure 1. Example of polar functional group (a) Epoxy, (b) BMI

In this work, we have successfully combined various low polarity materials to achieve an extremely low Df while simultaneously achieving good thermal and mechanical reliability performance. The key point for this technology is to combine different low polarity components that contribute to stronger mechanical and thermal performance. Even within the low polarity materials, some components have functional groups with good interaction between the materials (such as π π interaction by styrene group), some components have flexible structures (such as long alkyl chain etc.) resulting in better mechanical property, and some components form high density crosslinking yielding better thermal properties. Therefore, by optimizing the combination of these low polarity components, we could achieve extremely low Df materials that have both good mechanical and thermal performance.

Another important aspect of developing extremely low loss materials is Dk. Dk directly affects signal propagation speed and transmission line losses. Varying the Dk value (ε_r) in the formulas shown in Figure 2, we can establish dielectric thickness is reduced while maintaining a constant trace width, resulting in lower transmission loss and higher circuit density. Furthermore, since propagation speed is inversely proportional to Dk, low Dk materials are the key to higher signal speeds. We have investigated a low Dk filler that is optimal for the low loss materials.

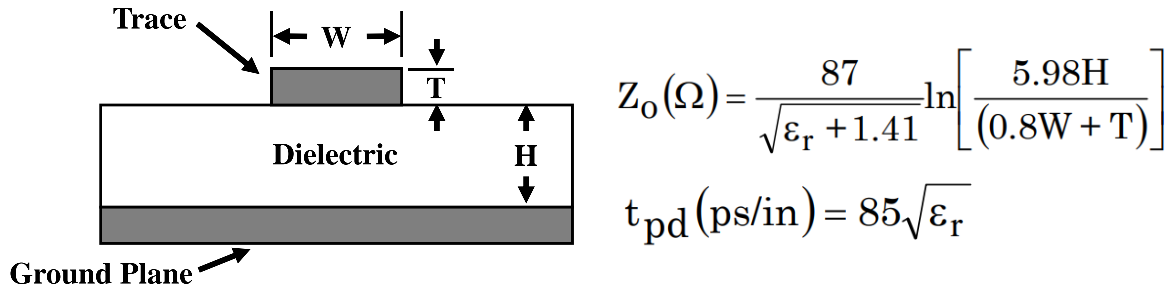


Figure 2. Dk effect on design and performance

PCB fabrication and assembly processes such as drilling, desmearing, and soldering apply mechanical, chemical, and thermal stress [2] to the material. These stresses may damage the material and cause defects like cracks or delamination between the laminate layers. It is necessary to check if the low polarity material has enough durability to withstand these steps. Therefore, PCB test vehicles were fabricated and evaluated for robustness and reliability. In addition to durability against stress, another important processability consideration for PCB materials is how easily the resulting debris can be removed after drilling. If the debris cannot be removed by desmear, it may cause interconnect defects (ICD) that could lead to failure of a circuit. Ultimately, building PCBs using multiple fabricators each with different manufacturing equipment, different processes, and different people, we can confirm the material is compatible with PCB processes.

Experimental Methodology

Laminate creation

Prepreg investigated in this study was made by coating on glass cloth. A curable composition was prepared by dissolving the soluble resin components in toluene. Insoluble silica and flame-retardant components were added and dispersed in the resin varnish using a rotor-stator mixer. A curable composition was poured into a grounded metal pan and a glass cloth was impregnated with the curable composition by pulling through a gap of metal bars having a controlled gap. The coating thickness was adjusted by gap width. The prepreg was dried with air flow at room temperature for 10 minutes and then heated up to 130°C to form a dried prepreg. Two layers of prepreg were laminated with 1/2 oz HVLP2 copper foil on both sides to form a laminate. The laminate was cured at 216 °C for 2 hours at 30 bars.

Resin Content (RC)

The weight of glass cloth was measured before it was coated with a curable composition. After coating and drying, the total weight of the prepreg thus formed was measured. RC was calculated based on the following equation:
RC = (Total prepreg weight – Glass cloth weight)/(Total prepreg weight)

Cu Peel Strength Test

Cu peel strength was measured based on 1/2 oz Cu weight per unit area using the IPC-TM-650 TEST METHODS MANUAL Peel Strength. United SSTM-1 Model was used for Cu peel strength measurement.

Inner Layer Bond Strength (ILBS) test

ILBS was measured based on IPC-TM650 2.4.40. It is similar test to Cu peel strength, but it evaluates resin-to-resin bonding strength (without Cu). United SSTM-1 Model was used for ILBS measurement. Specifically, a two-layer laminate with 2116NE glass cloth was used.

Dielectric Measurements

Dk and Df was measured using a Split Post Dielectric Resonator (QWED Technologies) at 10 GHz with an Agilent Technologies N5230A PNA Series Network Analyzer. Dk and Df against frequency were measured using Balanced Type Circular Disk Resonator (BCDR) (Keysight) at from 14GHz to around 100 GHz.

Thermal Measurements
Dimensional change and CTE was measured using TMA Q400 Thermomechanical Analyzer (TA Instruments). Data was collected from 40 to 300 °C. Weight loss was measured by TGA Q50 (TA instruments). Data was collected from 40 to 550 °C with 10°C/min heat rise rate. Tg was measured by DMA Q800 (TA instruments). The ratio of storage modulus against loss modulus was plotted and its peak was defined as Tg of the material. Data was collected from 40 to 300 °C with 5°C/min heat rise rate.

Particle size distribution
Particle size distribution of the resin varnish was evaluated by particle size analyzer (Malvern Instrument Ltd.).

Results and Discussion
To investigate the effect of introducing polar components into low polar resin, several resin combinations were evaluated. BMI and diacrylate resin were chosen as polar component additives. When polar components were introduced into low polar hydrocarbon thermoset resin, Cu peel strength and inter laminate bond strength (ILBS) tended to improve (especially for ILBS). These results imply that the interaction between the laminate and laminate was improved by incorporating the polar component. As Mixture E in Table 1 shows, the improvement on adhesion is not enough if the amount of non-polar resin is lacking. It was seen that poor compatibility between the resin components resulted in material breakage via interface during peel test or ILBS test. As the resin content (RC) of laminate varies from sample to sample, Df values were normalized by extrapolation to 100% resin. In all mixtures with polar components, the Df is much higher than Mixture A, which consists of only low polar resin. Therefore, to achieve an extremely low Df material, it is critical to avoid using polar components as much as possible.

Table1. Comparison of properties with/without polar component into low polar resin (laminate with 2116 NE glass)

	Mixture A	Mixture B	Mixture C	Mixture D	Mixture E
Low polar resin 1	100	80	80	80	85
Low polar resin 2				10	
BMI resin		20	20		10
Diacrylate resin				10	5
Peroxide	0.5	0.5		0.5	0.5
Cu peel strength (N/cm) 1/2 oz HVLP2 Cu	4.7	6.7	6.8	4.4	4.0
Inter laminate bond strength (N/cm)	2.5	4.7	5.1	5.1	3.3
Df values of the resin extrapolated from RC at 10 GHz by SPDR methods	0.0016	0.0023	0.0024	0.0022	0.0021

Within the low polarity materials, there are components that have relatively good thermal reliability and components that have relatively good mechanical reliability. The components with good thermal reliability contribute to high crosslink density, causing low CTE values. In contrast, the components with good mechanical reliability have flexible structures that contribute to toughness and adhesion. Utilizing only high thermal reliable components, yields a result that is too brittle. In contrast, if using only high mechanically reliable components, the crosslinking density becomes too low, yielding high CTE.

Good mechanical reliability
* Toughness
* Adhesion

Good thermal reliability
* Low CTE values
* Stable under process temperature (288 °C)

Figure 3. Concept of high reliability materials

Table 2 is the resulting summary of properties with different combinations of high and low polarity components. A to C all consist of low polar components with extremely low Df. A is the formulation with the highest amount of mechanically robust components; it has good ILBS suggesting good mechanical reliability against delamination during PCB process. In contrast, α1 value is very high, which could lead to cracks through continuous thermal excursions. Interconnect Stress Testing (IST) is one of the benchmarks to evaluate the thermal reliability of PCB materials by adding consecutive thermal excursions. Because

IST includes factors of the PCB process such as plated Cu quality [3], higher α1 values generally lead to failure [4]. Because of the high temperatures PCBs are exposed to during the solder reflow process, overall CTE including the temperature above Tg is another critical property to consider [5]. If the overall CTE is too high, there is the risk of delamination or cracks because of CTE mismatch between laminate and Cu. Thus, the CTE is a dependable general metric to gauge thermal reliability levels and board performance. B is the formulation incorporating a thermally robust component. It has good α1 and overall CTE, so it is considered to have good thermal reliability against thermal stress during PCB process and usage. In contrast, ILBS is very poor and there is high risk of delamination by mechanical stress like drilling during the PCB process. C is the formulation in which both thermally and mechanically robust components were appropriately combined. The properties of C show good balance between CTE and ILBS while maintaining an extremely low Df. These results suggest that thermal property and mechanical property can be balanced by the appropriate combination of low polarity components.

Table2. The component effect on the overall property

Discription		Reference Conventional low loss materials	A: Formulation with mechanically good component	B: Formulation with thermally good component	C: Formulation with optimal comnbination of mechanically good component and themally good component
TMA (2116 NE glass)	α1 mm/m°C	40	**<u>100</u>**	50	60
	Z-CTE overall, % 50-288°C	2.9	**<u>3.5</u>**	2.0	2.7
ILBS, N/cm (2116 NE glass)		5.4	5.8	**< <u>3.5</u>**	4.7
Df at 10GHz (1078 NE glass)		0.0019	0.0012	0.0010	0.0011

The signal integrity (SI) test of the extremely low loss material was evaluated using a 6 layers design for strip line methods. As Figure 4 shows, there is much lower loss in the extremely low loss material compared to the conventional low loss material. The loss at 28 GHz was -0.38 dB/cm for the conventional low loss material and -0.31 dB/cm for the extremely low loss material. It is around 20% improvement.

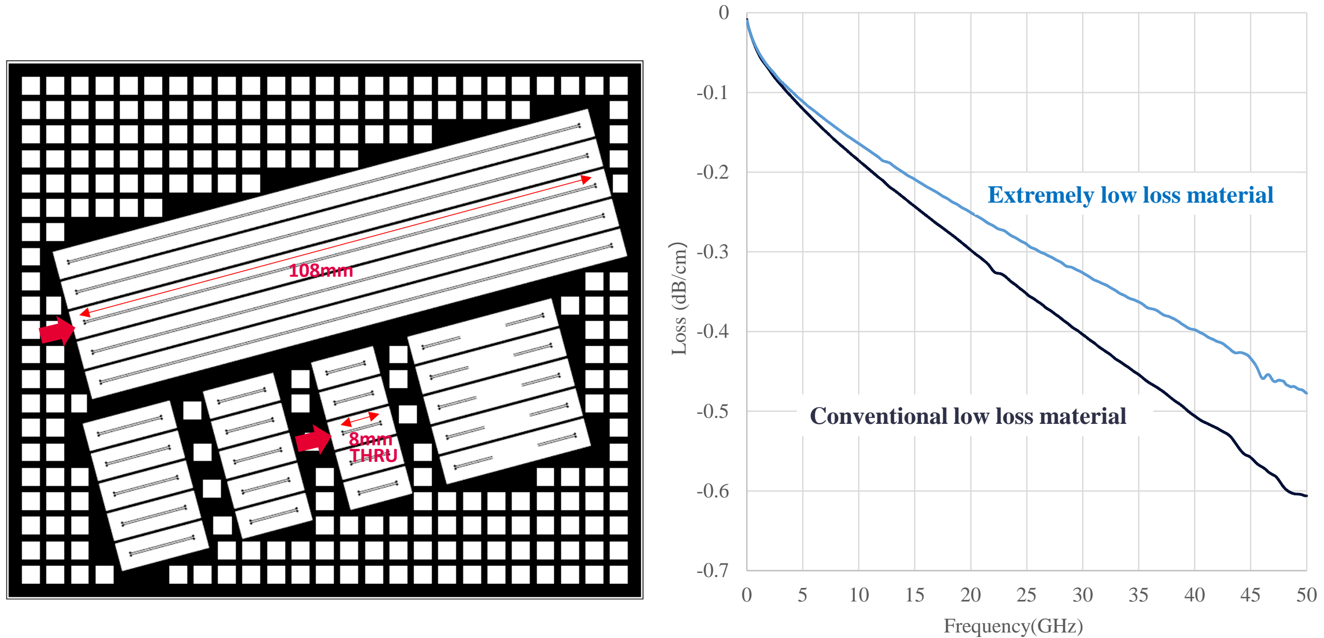


Figure 4. Insertion loss results by strip line methods.

In the next step, we proceeded with the evaluation of processability and reliability of the extremely low loss material by fabricating a PCB based on HDPUG industry standard MRT-7 (Material Reliability Test Version 7) procedure. MRT-7 is a generic material qualification test vehicle design and procedure, which is developed to enable specific survivability and reliability testing of bare board materials [3]. To date, more than 200 materials have been tested on various MRT versions. Although this test vehicle includes testing of assembly reflow survival, thermal analysis, IST, CAF, electrical, and more, it is not designed with consideration of advanced PCB technologies consisting of multiple laminations, build-up layers, or stacked microvias. The design was modified to include three laminations, stacked and staggered microvias, epoxy filled buried vias, and back-drilling. A 20-layer mixed resin content stack-up, which is recognized as more challenging to fabricate and pass

performance testing, was selected. The PCB stack-up and test coupon layout are shown in Figure 5 and Figure 6 respectively. NE glass was used for laminate and prepreg for the evaluation.

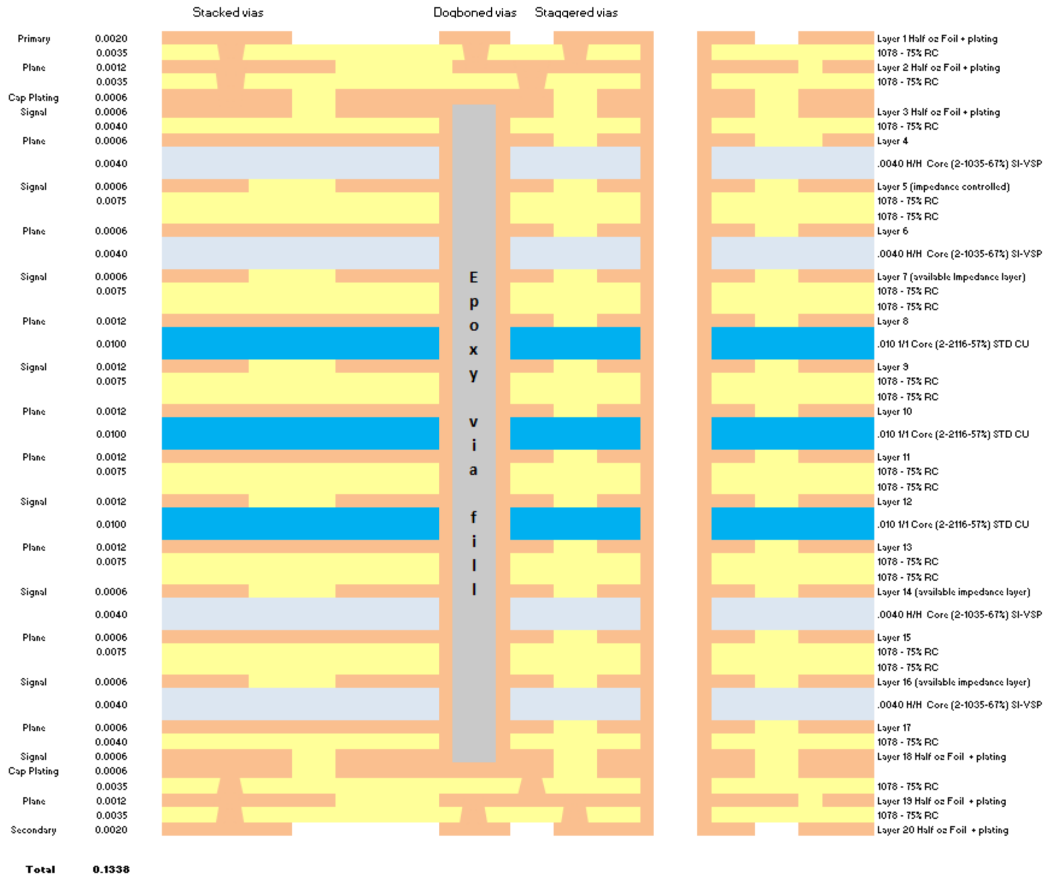


Figure 5. Stack up of the PCB for internal test

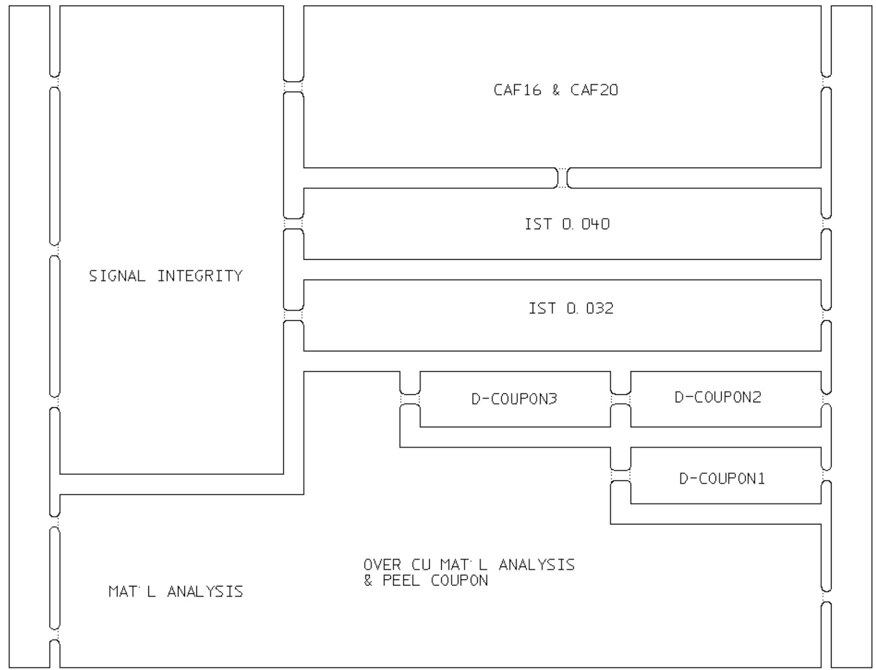


Figure 6. Design of the PCB and thickness of each part

PCBs used for electrical testing, IST, Thermal Analysis, CAF, and OM Thermal Stress (D-coupons) are tested as-received and with 6X lead-free assembly reflow temperature of 260°C preconditioning. The fabricator's cross-sectional image of through

holes after thermal stress is shown in Figure 7. There is no delamination between laminate/laminate or laminate/Cu, suggesting the material has good mechanical and thermal reliability. In addition, there are no interconnect defects (ICDs) suggesting the material is compatible with normal desmear processing. From the results, it is indicated that the extremely low loss material has good processability.

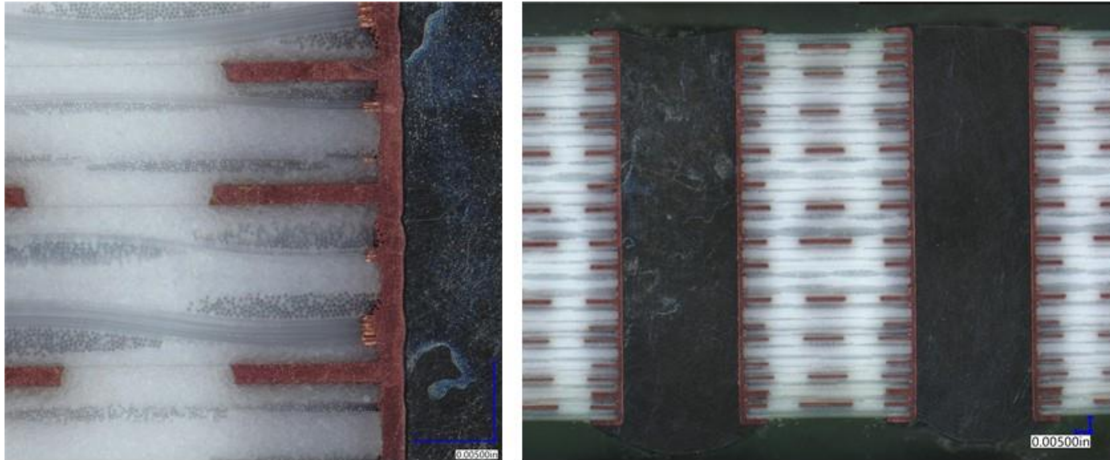


Figure 7. The cross-sectional image of through hole after thermal stress

We also evaluated the reliability using the PCB. Figure 8 shows IST result from 25℃ to 150℃. 1000 cycles were conducted for 0.8mm pitch and 1.0mm pitch with and without preconditioning. Preconditioning was done by six times reflow at 260℃. From the results, all sample passed 1000 cycles thermal stress with less than 10% resistance change criteria. The positive results suggest the material has good thermal reliability.

No preconditioned

	0.8mm pitch	1.0mm pitch
N1	1000 cycles Pass	1000 cycles Pass
N2	1000 cycles Pass	1000 cycles Pass
N3	1000 cycles Pass	1000 cycles Pass
N4	1000 cycles Pass	1000 cycles Pass
N5	1000 cycles Pass	1000 cycles Pass
N6	1000 cycles Pass	1000 cycles Pass

Preconditioned (6x reflow at 260°C)

	0.8mm pitch	1.0mm pitch
N1	1000 cycles Pass	1000 cycles Pass
N2	1000 cycles Pass	1000 cycles Pass
N3	1000 cycles Pass	1000 cycles Pass
N4	1000 cycles Pass	1000 cycles Pass
N5	1000 cycles Pass	1000 cycles Pass
N6	1000 cycles Pass	1000 cycles Pass

Figure 8. IST results of non-preconditioned and preconditioned coupons

Three D-coupon design variations consisting of two-stacked, dog-boned, and staggered microvias (via structure is described in Figure. 5) were added to the test vehicle. Drill diameter is 150 um, prepreg thickness is 90 um and aspect ratio is 1.7/1.0. The stacked microvias were offset from the buried via at 12 mils and 16 mil pitches. As Figure 9 shows, the material has excellent laser drilling processability. To check the thermal reliability of the microvias, D-coupon OM testing was conducted. The OM test plan and results of the microvia are shown in Figure 10 and Figure 11.

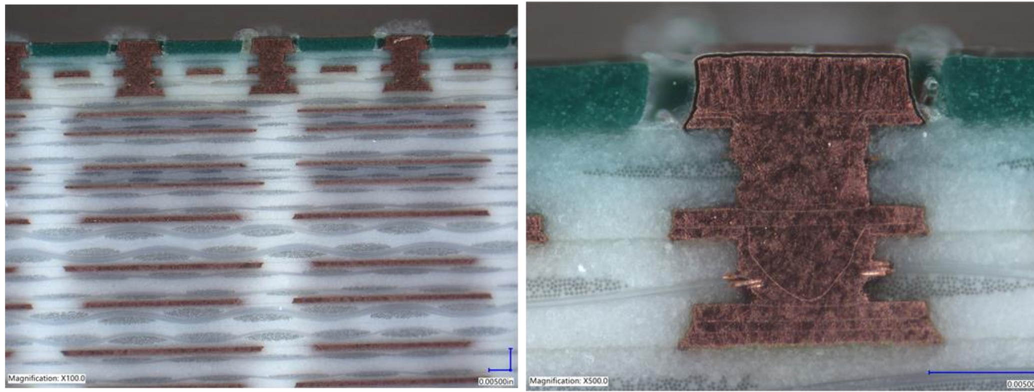


Figure 9. Cross-section images of microvias

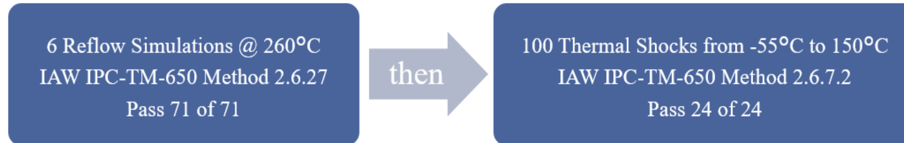


Figure 10. Test plan for D-coupon

Coupon Number (D1,D2,D3)	Reflow simulation (260°C)								Thermal shock (-55°C to 150°C)							
	Ref 260C - Nom RT Resistance (ohms)				Change after 6 cycles (%)				Ref 150C - Nom RT Resistance (ohms)				Change after 100 cycles (%)			
	Net 1D1	Net 2D1	Net 1D2	Net 1D3	Net 1D1	Net 2D1	Net 1D2	Net 1D3	Net 1D1	Net 2D1	Net 1D2	Net 1D3	Net 1D1	Net 2D1	Net 1D2	Net 1D3
1,9,17	1.019	0.837	0.971	0.542	0.1	0.2	-0.1	0.0	0.486	0.397	0.481	0.267	0.7	0.9	0.3	0.8
2,10,18	1.041	0.879	1.236	0.553	0.1	0.2	-0.3	0.1	0.502	0.422	0.497	0.275	0.7	0.9	0.3	0.7
3,11,19	1.046	0.871	1.026	0.530	0.1	0.2	-0.2	0.3	0.512	0.424	0.516	0.266	0.8	1.1	0.5	0.8
4,12,20	1.093	0.918	1.072	0.540	0.2	0.2	-0.2	0.3	0.540	0.432	0.538	0.273	1.0	1.2	0.6	0.9
5,13,21	1.061	0.831	1.061	0.531	0.2	0.2	-0.1	0.0	0.526	0.412	0.536	0.265	0.7	1.0	0.5	0.6
6,14,22	1.081	0.844	1.104	0.554	0.2	0.3	-0.2	0.0	0.540	0.422	0.548	0.270	0.7	0.9	0.5	0.7
7,15,23	1.064	0.851	1.127	0.576	0.1	0.2	-0.1	0.0	0.531	0.425	0.560	0.276	0.6	0.7	0.7	0.6
8,16,24	1.006	0.826	1.054	0.578	-0.1	0.0	0.1	0.1	0.498	0.407	0.521	0.275	0.5	0.6	0.7	0.9

Figure 11. D-coupon test results.
Net 1D1 is Dog-bone, Net 2D1 is Stacked, Net 1D2 is Staggered, Net 1D3 is Stacked
Nets 1D1, 2D1, 1D2 microvias are 12mils offset, 1D3 is 16mils offset from buried mechanical via

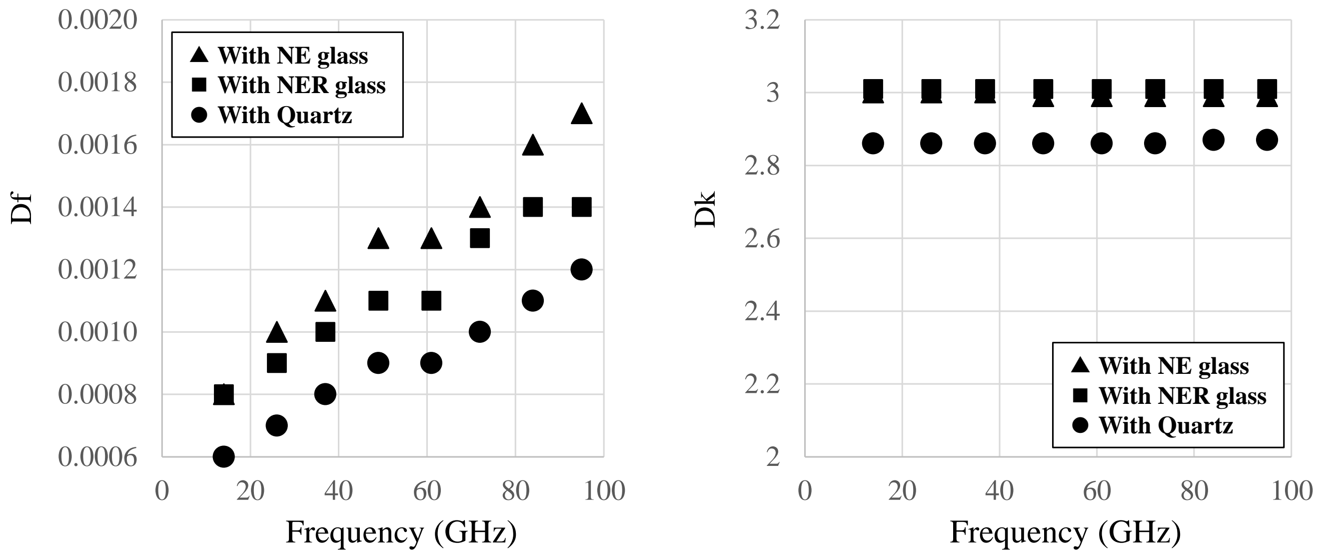
The thermal and mechanical properties of single lamination and three laminations is shown in Table 3. A slight increase in the glass transition temperature indicates further crosslinking occurred during multiple laminations. However, Z axis expansion values are very stable after preconditioning and multiple laminations, suggesting the materials were almost fully cured after one lamination and the effect of further curing is very small. In addition, 5% weight loss temperature by TGA is in the same range among all conditions. When materials are damaged by heating of preconditioning or multiple laminations, chemical bonds within resin systems begin to break and some amount of lower molecular weight components will be evaporated into gas [5], causing higher weight loss (= lower 5wt% loss temperature.). However, this material shows the same values even after three lamination and preconditioning, implying the materials are stable against heat during the lamination process.

Table 3. PCB properties after single and three laminations

Property	Condition	Single Lamination		Three Laminations		Unit	Test Method
		As Received Value	Precondtioned Value	As Received Value	Precondtioned Value		
Glass Transition Temperature (Tg)	DMA	194	196	198	199	°C	IPC-TM-650.2.4.24.3
Degradation Temperature (TGA)	Degradation Temp (TGA) (5% wt. loss)	376	373	377	376	°C	IPC-TM-650.2.3.40
Z Axis Expansion	50°C to 260°C	2.3	2.5	2.7	2.5	%	IPC-TM-650.2.4.24
Z Axis CTE Alpha 1 / Alpha 2	50°C to Tg / Tg to 260°C	76 / 215	78 / 233	78 / 251	75 / 209	ppm/°C	IPC-TM-650.2.4.24

From the results of PCB evaluation, it is determined that the extremely low loss material consisting of only low polar components has good processability, mechanical, and thermal reliability. The test results indicate the possibility of this material, which consists of only low polar components, is applicable for 112Gbs and 224Gbps application.

To further investigate lowering loss, we studied the effect of cloth on Df and Dk in different frequencies. We evaluated dielectric properties of the material with different cloth (NE, NER [6], Quartz) by Balanced Type Circular Disk Resonator (BCDR) methods, where Df and Dk were measured up to 100 GHz. The results are shown in Figure 12. Regardless of cloth, the extremely low loss material exhibited Df less than 0.001until 26Ghz. Upon applying quartz cloth, Df stays below 0.001 until 72 GHz. Df with quartz glass is approximately 30% lower than Df with standard fiberglass. Because dielectric loss is proportional to the Df values, this implies the type of cloth affects dielectric loss. Dk is lower when quartz cloth was applied to the material, showing evidence of improving loss reduction.



BCDR measurement
Sample construction: 1078 2ply
Sample thickness: 4.5±0.3 mil

Figure 12. Df and Dk frequency dependency of the material with different cloth

For further loss reduction, we investigated approaches to reduce Dk. Most PCB materials employ inorganic fillers like silica to balance the thermal and mechanical property. The Dk of silica and quartz is around 3.7-4.0. However, low polar organic materials usually have less than 3.0 of Dk. Therefore, the dominant factor that decides the total Dk value is the filler. In recent years, hollow fillers, in which air is introduced into the inorganic filler to lower the Dk, have been introduced into the market. Table4 is the example of available hollow fillers. Compared with solid silica, Dk of hollow filler is effectively reduced in all products. Because Df is relatively higher in hollow glass, we used hollow silica for further investigation.

Table 4. Silica and hollow filler summary

Material Type	Structure	Size D_{50} (μm)	D_{max} (μm)	Density (g/mL)	Dk	Df
Amorphous Silica	Solid	0.5 - 3	<10	2.2	4	0.0006-0.001
Amorphous Silica	Hollow	2	<10	0.5	1.5	0.001
Soda-lime-borosilicate glass	Hollow	20	>20	0.5	1.5	0.005
Alumina borosilicate glass	Hollow	4	>10	0.6	1.8	0.003

We introduced the hollow silica into our extremely low loss material formulation and made the laminate sample. To avoid breakage of the hollow silica particles, high shear mixing was used before incorporating hollow silica into the varnish. We checked the particle size by particle size analyzer to make sure hollow silica was dispersed evenly without high sheer mixer.

244 The measured values of D50 and D90 were 2.4 um and 6.7 um respectively, suggesting the hollow silica was dispersed very
245 well into the low polar matrix. To make sure hollow silica is dispersed in both the varnish and cured laminate, we also checked
246 cross sectional images of the laminate. Figure 13 is a cross-sectional image of a laminate made with the material containing
247 hollow silica. The cross-sectional image suggests that dispersity of hollow silica is good and hollow silica particles existed
248 without breaking after exposure to high pressure during the lamination process.
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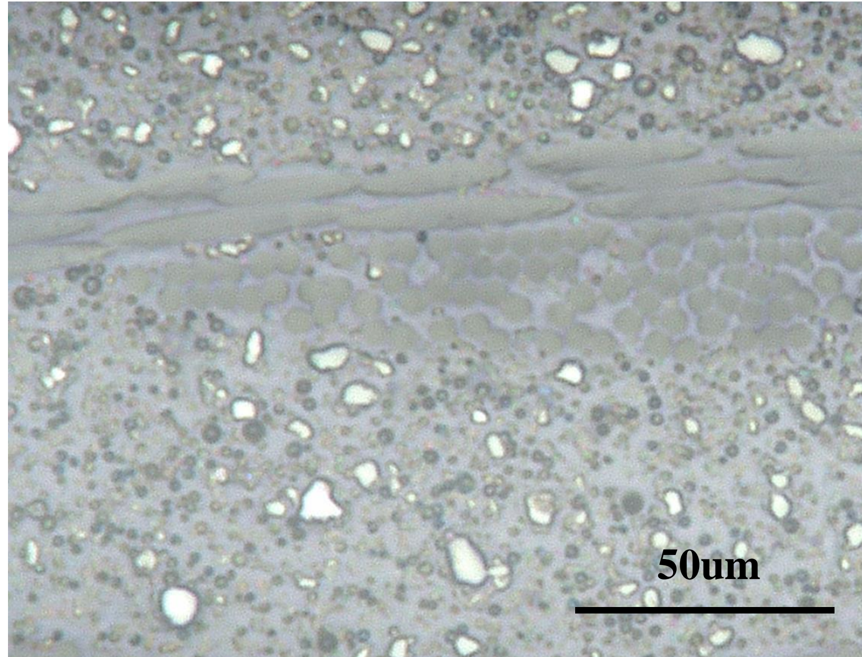

250
251 **Figure 13. Cross sectional image of laminate with hollow silica**
252
253 Df and Dk values were evaluated by BCDR methods. The results of the formulation with the hollow silica replacement are
254 shown below. Dk values are effectively lowered by introducing hollow silica. All samples show Dk less than 2.6 regardless
255 of the cloth and the values are stable against frequency change. Df values tend to be a bit higher than the formulation with
256 solid silica. This may be because hollow silica has higher surface area from higher porosity compared to regular silica. The
257 surface of the silica has the hydrophilic chemical structure of silanol and more silanol remains in hollow silica than solid silica.
258 However, Df values still maintain low levels until higher frequency. From the results, we can achieve Df = 0.0010 to 0.0011
259 with Dk lower than 2.6 at 28GHz with all cloth types employed. The combination of this level of low Df and low Dk is
260 considered to meet 224 Gbps requirement. We are planning to further investigate the effect of both Dk and Df to further reduce
261 loss. We are also planning to evaluate the processability like drilling of the materials with hollow silica.
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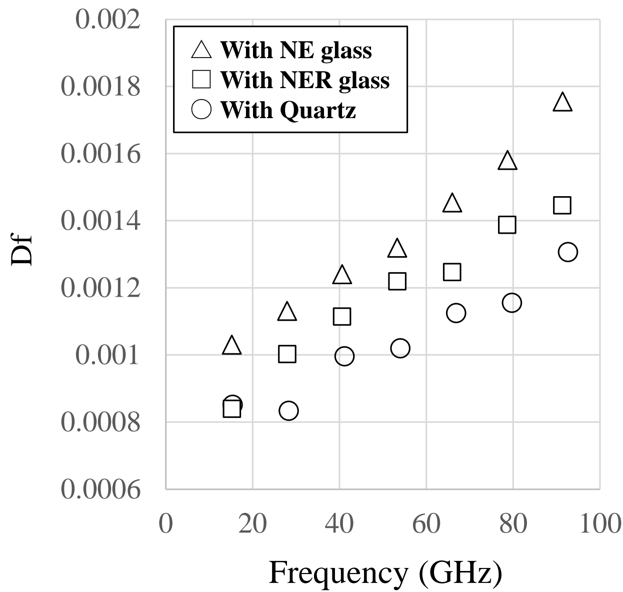

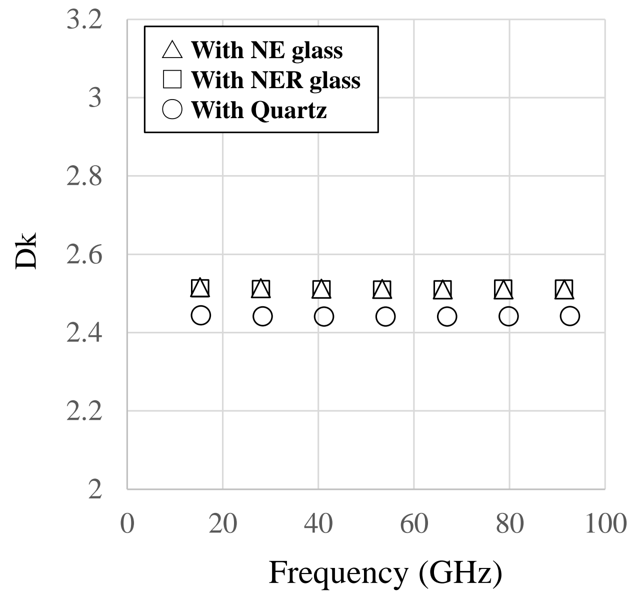

BCDR measurement
Sample construction: 1078 2ply
Sample thickness: 4.5±0.3 mil

Figure 14. Df and Dk frequency dependency of the material with hollow silica replacement

Conclusions

This paper investigated how to achieve extremely low loss materials with good survivability of PCB processes. The effect of polar components was discussed, and it was revealed that the increase in Df by incorporation of polar component is not neglectable for achieving extremely low loss materials. We successfully balanced the overall properties by combining an appropriate combination of low polar component. Adding both thermally and mechanically reliable components into a low polarity resin was key for achieving our target properties. Signal integrityperformance was also greatly improved compared with conventional low loss materials. We have verified the applicability of the extremely low loss material for PCB application by utilizing MRT-7 based PCB test vehicle enhanced with features of advanced PCB technologies. The extremely low loss material that consists of only low polar components showed good processability and reliability for actual PCB process. Further possibility to lower Df and Dk was investigated by substituting cloth and fillers. Df could be controlled to less than 0.001 by changing the cloth and Dk could be controlled down to less than 2.6 by usage of hollow fillers. From these results, the extremely low loss material is considered capable of supporting 112/224Gbps PCB applications.

Acknowledgements

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